

PHILIPS

Data handbook



Electronic
components
and materials

Semiconductors

Book S5

1988

Small-signal field-effect transistors

SMALL-SIGNAL FIELD-EFFECT TRANSISTORS

page

Selection guide

N-channel junction field-effect transistors	
general purpose	5
differential amplifiers	7
switching	8
P-channel junction field-effect transistors	
switching	9
N-channel MOSFETs	
single gate (switching)	10
dual gate (VHF/UHF)	11
N-channel vertical D-MOSFETs	12
P-channel vertical D-MOSFETs	13

Type number survey (alphanumerical)	17
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General

Type designation	23
Rating systems	25
s-parameters	27
TO-92 variant transistors on tape	29
Tape and reel specification SOT-23, SOT-89 and SOT-143	33
Soldering recommendations SOT-23, SOT-143 and SOT-89	37
Soldering recommendations SOT-103	41
Thermal characteristics SOT-23 and SOT-143 envelopes	43

Device data

Junction FETs	49
MOSFETs single gate	195
MOSFETs dual gate	227
Vertical D-MOSFETs	305

Accessories	384
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Semiconductor index relating to all Semiconductor Devices Handbooks	385
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SELECTION GUIDE

N-channel junction field-effect transistors, general purpose

type number	envelope	RATINGS		CHARACTERISTICS						remarks	page
		$\pm V_{DS}$	I_G	I_{DSS} min.-max.	$-V_{(P)GS}$ max.	$ v_{fs} $ min. $f = 1 \text{ kHz}$	C_{rs} typ.				
		V	mA	mA	V	mS	pF				
BC264A	TO-92 var.	30	10	2,0-4,5	> 0,5	2,5	1,2	hi-fi amplifiers and a.f. equipment		49	
BC264B				3,5-6,5		3,0				49	
BC264C				5,0-8,0		3,5				49	
BC264D				7,0-12,0		4,0				49	
BF245A	TO-92 var.	30	10	2,0-6,5	8,0	3,0-6,5	1,1	d.c., l.f. and h.f. amp.		55	
BF245B				6-15						55	
BF245C				12-25						55	
BF247A	TO-92 var.	25	10	30-80	0,6-14,5	8	3,5	v.h.f. and u.h.f. amp. general purpose sw.		67	
BF247B				60-140						67	
BF247C				110-250						67	
BF256A				3-7						69	
BF256B	TO-92 var.	30	10	6-13	7,5	4,5	0,7	v.h.f. and u.h.f. appl.		69	
BF256C				11-18						69	
BF410A	TO-92 var.	20*	10	0,7-3,0	typ. 0,8	2,5	0,3	r.f. stages f.m. portables r.f. stages car radios r.f. stages mains radios mixer stages		81	
BF410B				2,5-7,0		4,0				81	
BF410C				6-12		6,0				81	
BF410D				10-18		7,0				81	
BF510	SOT-23	20	10	0,7-3,0	typ. 0,8	2,5	0,3	r.f. stages f.m. portables r.f. stages car radios r.f. stages mains radios mixer stages		85	
BF511				2,5-7,0		4,0				85	
BF512				6-12		6,0				85	
BF513				10-18		7,0				85	
BFR30	SOT-23	25	5	4-10	5	1,0-4,0	0,85	low-level general purpose amplifiers		99	
BFR31				1-5		2,5				1,5-4,5	99
BFR101A	SOT-143	30	10	0,2-1,5	1,0	1,2	—	source follower		109	
BFR101B				1-5		2,5				2,5	109

* Asymmetrical.

N-channel junction field-effect transistors, general purpose

type number	envelope	RATINGS		CHARACTERISTICS						remarks	page
		$\pm V_{DS}$	I_G	I_{DSS} min.-max.	$-V(P)GS$ max.	$ y_{fs} $ min. $f = 1 \text{ kHz}$	C_{rs} typ.				
		V	mA	mA	V	mS	pF				
BFT46	SOT-23	25	5	0,2-1,5	1,2	1,0	0,85		general purpose ampl.	117	
BFW10	TO-72	30	10	8-20	8	3,5-6,5	0,6		broad band up to 300 MHz and differential ampl.	125	
BFW11				4-10	6	3,0-6,5				125	
BFW12	TO-72	30	5	1-5	2,5	2,0	0,6		low current-low voltage applications	137	
BFW13				0,2-1,5	1,2	1,0				137	
BFW61	TO-72	25	10	2-20	8	2,0-6,5	$< 2,0$		general purpose ampl.	147	
2N3822	TO-72	50	10	2-10	6	3,0-6,5	$< 3,0$		general purpose h.f. ampl.	173	
2N3823	TO-72	30	10	4-20	8	3,5-6,5	$< 2,0$		industrial i.f./r.f. ampl.	175	

N-channel junction field-effect transistors for differential amplifiers

type	RATINGS			CHARACTERISTICS														
	individual transistor		total device	individual transistor		total device												
	$\pm V_{DS}$ V	I_G mA	I_G mA	I_{DSS} min. max. mA	$-V_{(P)GS}$ min. max. V	$ \Delta V_{GS} $ max. mV	$\left \frac{d\Delta V_{GS}}{dT}\right $ max. $\mu V/K$	$\left \Delta \frac{1}{g_{fs}}\right $ max. Ω	$\left \Delta \frac{g_{os}}{g_{fs}}\right $ max. $\mu V/V$	CMRR min. dB	page							
BFQ10 BFQ11 BFQ12 BFQ13 BFQ14 BFQ15 BFQ16	TO-71	30	—	10	0,5 10	0,5 3,5	5 10 10 10 15 20 50	5 5 10 20 20 40 50	6 6 12 12 12 20 30	10 30 30 30 30 30 100	100 90 90 90 90 90 80	91 91 91 91 91 91 91						
BFS21 BFS21A							SOT-52	30	10	0,5	1 —	— 6	20 10	75 40	15 7,5	1000 500	60 66	111 111

N-channel junction field-effect transistors for switching

type number	envelope	RATINGS		CHARACTERISTICS								page
		V _{DS} V	I _G mA	I _{DSS} min. mA	I _{DSS} max. mA	-V(P) _{GS} min. V	r _{ds on} max. Ω	C _{rs} max. pF	t _{on} max. ns	t _{off} max. ns		
BSR56	SOT-23	40	50	50	—	4	10	25	5	9	25	153
BSR57				20	100	2	6	40		10	50	153
BSR58				8	80	0,8	4	60		20	100	153
BSV78	TO-18	40	50	50	—	3,75	11	25	5	10	10	161
BSV79				20	—	2	7,0	40		18	16	161
BSV80				10	—	1	5,0	60		30	32	161
PMBF4391	SOT-23	40	50	50	150	4	10	30	3,5	15	20	169
PMBF4392		40		25	75	2	5	60		15	35	169
PMBF4393		40		5	30	0,5	3	100		15	50	169
2N3966	TO-72	30	10	2	—	4	6	220	1,5	120	100	177
2N4091	TO-18	40	10	30	—	5	10	30	5	25	40	181
2N4092				15	—	2	7,0	50		35	60	181
2N4093				8	—	1	5,0	80		60	80	181
2N4391	TO-18	50	50	50	150	4	10	30	3,5	15	20	185
2N4392				25	75	2	5,0	60		15	35	185
2N4393				5	30	0,5	3,0	100		15	50	185
2N4856	TO-18	40	50	50	—	4	10	25	8	9	25	189
2N4857		40		20	100	2	6	40		10	50	189
2N4858		40		8	80	0,8	4	60		20	100	189
2N4859		30		50	—	4	10	25		9	25	189
2N4860		30		20	100	2	6	40		10	50	189
2N4861		30		8	80	0,8	4	60		20	100	189

P-channel junction field-effect transistors for switching

type number	envelope	RATINGS		CHARACTERISTICS							page
		$\pm V_{DS}$ V	I_G mA	I_{DSS} min. mA	I_{DSS} max. mA	$-V_{(P)GS}$ min. V	$R_{DS\ on}$ max. Ω	C_{rs} max. pF	t_{on} max. ns	t_{off} max. ns	
BSJ174	TO-92	30	50	20	135	5	85		7	15	149
BSJ175				7	70	3	125		15	30	149
BSJ176				2	35	1	250	4	35	35	149
BSJ177				1,5	20	0,8	300	2,25	45	40	149
BSR174	SOT-23	30	50	20	135	5	85		7	15	157
BSR175				7	70	3	125		15	30	157
BSR176				2	35	1	250	4	35	35	157
BSR177				1,5	20	0,8	300	2,25	45	45	157

N-channel MOS-FETs single gate for switching

type number	envelope	RATINGS		CHARACTERISTICS						page
		V _{DS} V	I _D mA	I _{DSS} min. mA	-V(P)G ^{**} V	mode	r _{DS} on max. Ω	C _{rs} typ. pF	t _{on} /t _{off} typ. ns	
BFR29	TO-72	30*	20	10 - 40	0,5 - 3,5	depl	-	0,4	-	195
BSD10	TO-72	10	50	-	2	depl	30	0,6	1/5	203
BSD12		20								203
BSD20	SOT-143	10	50	-	2	depl	30	0,6	1/5	207
BSD22		20								207
BSD212	TO-72	10	50	-	0,1 - 2	enh	70	0,6	1/5	211
BSD213		10								211
BSD214		20								211
BSD215		20								211
BSS83	SOT-143	10	50	-	0,1 - 2	enh	45	0,6	1/5	215
BSV81	TO-72	30*	25	-	-	depl	100	0,5	-	219

* V_{DB}/V_{SB}** enh. types V_{GS}(th)

N-channel MOS-FETS, Dual gate

type number	envelope	RATINGS		CHARACTERISTICS							remarks	page
		V _{DS}	I _D	I _{DSS} min. max. mA	-V(p)G1-S max. V	v _{fs} f = 1 kHz min. mS	C _{is} typ.	C _{os} typ.	F typ. dB			
		V	mA									
BF960*	SOT-103	20	20	2 20	3,5	9,5	1,8	0,9	2,8	UHF	227	
BF964*	SOT-103	20	30	2 20	2,5	15	2,5	1,0	1,5	VHF	231	
BF964S*	SOT-103	20	50	4 20	2,5	15	2,5	1,0	1,0	VHF	235	
BF965*	SOT-103	20	30	2 20	2,5	15	2,5	1,0	1,0	VHF	241	
BF966*	SOT-103	20	30	2 20	2,5	15	2,2	0,8	2,8	UHF	245	
BF966S*	SOT-103	20	30	4 20	2,5	15	2,3	0,8	1,8	UHF	249	
BF980*	SOT-103	18	30	—	1,3	17	2,6	1,1	2,8	UHF	255	
BF981*	SOT-103	20	20	4 25	2,5	10	2,1	1,1	1,0	VHF	259	
BF982*	SOT-103	20	40	—	1,3	20	4,0	2,0	1,2	VHF	267	
BF989*	SOT-143	20	20	2 20	2,7	9,5	1,8	0,9	2,8	UHF	271	
BF990*	SOT-143	18	30	—	1,3	17	2,6	1,2	2,8	UHF	273	
BF991*	SOT-143	20	20	4 25	2,5	10	2,1	1,1	1,0	VHF	277	
BF992*	SOT-143	20	40	—	1,3	20	4,0	2,0	1,2	VHF	279	
BF994*	SOT-143	20	30	2 20	2,5	15	2,5	1,0	1,5	VHF	281	
BF994S*	SOT-143	20	50	4 20	2,5	15	2,5	1,0	1,0	VHF	285	
BF996*	SOT-143	20	30	2 20	2,5	15	2,2	0,8	2,8	UHF	287	
BF996S*	SOT-143	20	30	4 20	2,5	15	2,3	0,8	1,8	UHF	291	
BF997*	SOT-143	20	30	2 20	2,5	15	2,5	1,0	1,0	VHF	293	
BF984*	TO-72	20	50	20 55	3,8	12	5,5	3,5	2,3	General purpose	297	

* Protected against excessive input voltage surges.

N-channel vertical D-MOSFETs for switching

type number	envelope	RATINGS			CHARACTERISTICS						page
		V _{DS} V	I _D mA	P _{tot} at T _{amb} mW °C	V _{GS} (th) V	R _{DSon} typ. Ω max. Ω	I _D mA @ V _{GS} V	t _{on} /t _{off} max. ns			
BS107	TO-92 var.	200	120	500 25	1,8 (typ.)	15 28	20	2,6	10/10	305	
BS170	TO-92 var.	60	500	830 25	0,8-3,0	2,5 5	200	10	10/10	309	
BS170A	TO-92 var.	80	500	1000 25	1,5-3,5	2 4	500	10	10/15	317	
BS172A	TO-92 var.	80	300	830 25	1,5-3,5	7 10	150	5	10/10	321	
BS174A	TO-92 var.	200	300	1000 25	0,8-2,8	6 12	250	10	10/25	325	
BS176A	TO-92 var.	180	300	1000 25	0,7-2,7	7 10	15	3	10/15	329	
BS178	TO-126	450	750	15000 75*	2,0-4,0	10 14	100	10	10/100	333	
BS180	SOT-89	80	500	1000 25	1,5-3,5	2 4	500	10	10/15	337	
BS182	SOT-23	80	175	300 25	1,5-3,5	7 10	150	5	10/10	341	
BS184	SOT-89	200	250	1000 25	0,8-2,8	6 12	250	10	10/25	345	
BS186	SOT-89	180	300	1000 25	0,7-2,7	7 10	15	3	10/15	349	
BS195	TO-39	200	2000	10000 25*	1-3	1,8 2	1500	10	10/25*	353	
BS197	TO-18	180	300	1500 25*	0,7-2,7	7 10	15	3	10/15	357	
PH6659	TO-92 var.	35	750	1000 25	0,8-2,0	1,5	300	5	10/10	377	
PH6660		60	500			1,8	300	5		377	
PH6661		90	500			2,4	300	5		377	
2N6659	TO-39	35	1400	6250 25*	0,8-2,0	1,5 5	300	5	10/20	381	
2N6660	TO-39	60	1100	6250 25*	0,8-2,0	1,8 5	300	5	10/20	381	
2N6661	TO-39	90	900	6250 25*	0,8-2,0	2,4 5,3	300	5	10/20	381	

* T_{mb}

P-channel vertical D-MOSFETs for switching

type number	envelope	RATINGS			CHARACTERISTICS						page
		V _{DS} V	I _D mA	P _{tot} at T _{amb} mW °C	V _{GS} (th) V	R _{DSon} typ. Ω	max. Ω	I _D mA	@ V _{GS} V	t _{on} /t _{off} typ. ns	
BS250	TO-92 var.	45	250	830 25	1-3,5	9	14	200	10	4/10	313
BST100	TO-92 var.	60	300	1000 25	1,5-3,5	4,5	6	200	10	4/20	361
BST110	TO-92 var.	50	300	830 25	1,5-3,5	7,5	10	200	10	4/20	365
BST120	SOT-89	60	300	1000 25	1,5-3,5	4,5	6	200	10	4/20	369
BST122	SOT-89	50	250	1000 25	1,5-3,5	7,5	10	200	10	4/20	373

TYPE NUMBER SURVEY

In this alphanumeric list we present all field-effect transistors mentioned in this handbook.

type number	envelope	$\pm V_{DS}$ max. V	I_{DSS} mA	application	page
BC264A	TO-92 var.	30	2,0 - 4,5	hi-fi amplifiers and a.f. equipment	49
BC264B			3,5 - 6,5		49
BC264C			5,0 - 8,0		49
BC264D			7,0 - 12,0		49
BF245A	TO-92 var.	30	2,0 - 6,5	d.c., l.f. and h.f. amplifiers	55
BF245B			6,0 - 15,0		55
BF245C			12 - 25		55
BF247A	TO-92 var.	25	30 - 80	v.h.f. and u.h.f. ampl. general purpose switch	67
BF247B			60 - 140		67
BF247C			110 - 250		67
BF256A	TO-92 var.	30	3 - 7	v.h.f. and u.h.f.	69
BF256B			6 - 13		69
BF256C			11 - 18		69
BF410A	TO-92 var.	20*	0,7 - 3,0	r.f. stages f.m. portables	81
BF410B			2,5 - 7,0	r.f. stages car radios	81
BF410C			6 - 12	r.f. stages mains radios	81
BF410D			10 - 18	mixer stages	81
BF510	SOT-23	20	0,7 - 3,0	r.f. stage f.m. portables	85
BF511			2,5 - 7,0	r.f. stage car radios	85
BF512			6 - 12	r.f. stage mains radios	85
BF513			10 - 18	mixer stages	85
BF960	SOT-103	20	2 - 20	r.f. stage UHF TV tuner	227
BF964	SOT-103	20	2 - 20	r.f./mixer stage VHF TV tuner	231
BF964S	SOT-103	20	4 - 20	v.h.f. applications in TV tuner	235
BF965	SOT-103	20	2 - 20	v.h.f. TV tuner	241
BF966	SOT-103	20	2 - 20	r.f. stage UHF TV tuner	245
BF966S	SOT-103	20	4 - 20	v.h.f. applications	249
BF980	SOT-103	18	—	r.f. stage UHF TV tuner	255
BF981	SOT-103	20	4 - 25	r.f./mixer stage VHF TV tuner	259
BF982	SOT-103	20	—	r.f./mixer stage VHF TV tuner and FM radio tuner	267
BF989	SOT-143	20	2 - 20	u.h.f. TV tuners	271
BF990	SOT-143	18	—	u.h.f. TV tuners	273
BF991	SOT-143	20	4 - 25	v.h.f. TV and f.m. tuners	277
BF992	SOT-143	20	—	v.h.f. TV and f.m. tuners	279
BF994	SOT-143	20	2 - 20	u.h.f./v.h.f. TV tuners	281
BF994S	SOT-143	20	4 - 20	v.h.f. TV tuners	285
BF996	SOT-143	20	2 - 20	u.h.f. TV tuners	287
BF996S	SOT-143	20	4 - 20	u.h.f. TV tuners	291
BF997	SOT-143	20	2 - 20	u.h.f./v.h.f. TV tuners	293

* Asymmetrical.

** V_{DB} .

TYPE NUMBER SURVEY

type number	envelope	$\pm V_{DS}$ max V	I_{DSS} mA	application	page
BFQ10	TO-71	30	0,5 - 10	low level differential amplifiers	91
BFQ11					91
BFQ12					91
BFQ13					91
BFQ14					91
BFQ15					91
BFQ16					91
BFR29	TO-72	30**	10 - 40	v.h.f./low leakage/low noise	195
BFR30	SOT-23	25	4 - 10	general purpose amplifiers	99
BFR31			1 - 5		99
BFR84	TO-72	20	20 - 55	general industrial	297
BFR101A	SOT-143	30	0,2 - 1,5	source follower	109
BFR101B			1,0 - 5,0		109
BFS21	SOT-52	30	> 1	low level differential amplifiers	111
BFS21A					111
BFT46	SOT-23	25	0,2 - 1,5	general purpose amplifiers	117
BFW10	TO-72	30	8 - 20	wide-band up to 300 MHz and differential amplifiers	125
BFW11			4 - 10		125
BFW12	TO-72	30	1 - 5	low current-low voltage	137
BFW13			0,2 - 1,5		137
BFW61	TO-72	25	2 - 20	general purpose	147
BS107	TO-92 var.	200	< 0,03	relay and line-transformer	305
BS170	TO-92 var.	60	< 0,5 μA	drivers	309
BS250	TO-92 var.	45	< 0,5 μA	drivers	313
BSD10	TO-72	10	—	switch/convertor/chopper	203
BSD12		20	—		203
BSD20	SOT-143	10	—	switch/convertor/chopper	207
BSD22		20	—		207
BSD212	TO-72	10	—	switch/convertor/chopper	211
BSD213		10	—		211
BSD214		20	—		211
BSD215		20	—		211
BSJ174		TO-92	30		20 - 135
BSJ175	7 - 70			149	
BSJ176	2 - 35			149	
BSJ177	1,5 - 20			149	
BSR56	SOT-23	40	> 50	switch/chopper	153
BSR57			20 - 100		153
BSR58			8 - 80		153
BSR174			20 - 135		157
BSR175	SOT-23	30	7 - 70	switch/chopper	157
BSR176			2 - 35		157
BSR177			1,5 - 20		157
BSS83	SOT-143	10	—	switch/switch driver	215

* I_{Dmax} (A).

** V_{DB} .

type number	envelope	$\pm V_{DS}$ max. V	I_{DSS} mA	application	page
BST70A	TO-92 var.	80	0,5		317
BST72A	TO-93 var.	80	0,3	high-speed relay and	321
BST74A	TO-92 var.	200	0,3	line transformer driver	325
BST76A	TO-92 var.	180	0,3	in telephone circuits	329
BST78	TO-202	450	0,75		333
BST80	SOT-89	80	0,5*	} relay, high-speed and line-transformer drivers	337
BST82	SOT-23	80	0,175*		341
BST84	SOT-89	200	0,25		345
BST86	SOT-89	180	0,3*		349
BST95	TO-39	200	< 10,000	motor control	353
BST97	TO-18	180	0,3		357
BST100	TO-92 var.	60	0,3	relay, high-speed and	361
BST110	TO-92 var.	50	0,25	line-transformer drivers	365
BST120	SOT-89	60	0,3		369
BST122	SOT-89	50	0,25		373
BSV78			> 50		161
BSV79	TO-18	40	> 20	switch	161
BSV80			> 10		161
BSV81	TO-72	30	—	switch-chopper	219
PH6659		35			377
PH6660	TO-92 var.	60	< 10,000	inverter/driver	377
PH6661		90			377
PMBF4391			> 40		169
PMBF4392	SOT-123	40	> 25	switch/chopper	169
PMBF4393			> 5		169
2N3822	TO-72	50	2-10	general purpose h.f. ampl.	173
2N3823	TO-72	30	4-20	industrial i.f./r.f. ampl.	175
2N3966	TO-72	30	> 2	low power switch	177
2N4091			> 30		181
2N4092	TO-18	40	> 15	low power switch	181
2N4093			> 8		181
2N4391			> 50		185
2N4392	TO-18	40	> 25	low power switch/chopper	185
2N4393			> 5		185
2N4856		40	> 50		189
2N4857		40	> 20		189
2N4858		40	> 8		189
2N4859	TO-18	30	> 50	low power switch/chopper	189
2N4860		30	> 20		189
2N4861		30	> 8		189
2N6659		35	1,4*		381
2N6660	TO-39	60	1,1*	H.F. inverters and line drivers	381
2N6661		90	0,9*		381

* I_{Dmax} (A).

GENERAL

Type designation

Rating systems

s-parameters

TO-92 variant transistors on tape

**Tape and reel specification for
SOT-23, SOT-143 and SOT-89**

**Soldering recommendations for
SOT-23, SOT-143 and SOT-89**

**Soldering recommendations for
SOT-103**

**Thermal characteristics for
SOT-23 and SOT-143**

PRO ELECTRON TYPE DESIGNATION CODE FOR SEMICONDUCTOR DEVICES

This type designation code applies to discrete semiconductor devices — as opposed to integrated circuits —, multiples of such devices and semiconductor chips.

“Although not all type numbers accord with the Pro Electron system, the following explanation is given for the ones that do.”

A basic type number consists of:

TWO LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST LETTER

The first letter gives information about the material used for the active part of the devices.

- A. GERMANIUM or other material with band gap of 0,6 to 1,0 eV.
- B. SILICON or other material with band gap of 1,0 to 1,3 eV.
- C. GALLIUM-ARSENIDE or other material with band gap of 1,3 eV or more.
- R. COMPOUND MATERIALS (e.g. Cadmium-Sulphide).

SECOND LETTER

The second letter indicates the function for which the device is primarily designed.

- A. DIODE; signal, low power
- B. DIODE; variable capacitance
- C. TRANSISTOR; low power, audio frequency ($R_{th j-mb} > 15 \text{ K/W}$)
- D. TRANSISTOR; power, audio frequency ($R_{th j-mb} \leq 15 \text{ K/W}$)
- E. DIODE; tunnel
- F. TRANSISTOR; low power, high frequency ($R_{th j-mb} > 15 \text{ K/W}$)
- G. MULTIPLE OF DISSIMILAR DEVICES — MISCELLANEOUS; e.g. oscillator
- H. DIODE; magnetic sensitive
- L. TRANSISTOR; power, high frequency ($R_{th j-mb} \leq 15 \text{ K/W}$)
- N. PHOTO-COUPLER
- P. RADIATION DETECTOR; e.g. high sensitivity phototransistor
- Q. RADIATION GENERATOR; e.g. light-emitting diode (LED)
- R. CONTROL AND SWITCHING DEVICE; e.g. thyristor, low power ($R_{th j-mb} > 15 \text{ K/W}$)
- S. TRANSISTOR; low power, switching ($R_{th j-mb} > 15 \text{ K/W}$)
- T. CONTROL AND SWITCHING DEVICE; e.g. thyristor, power ($R_{th j-mb} \leq 15 \text{ K/W}$)
- U. TRANSISTOR; power, switching ($R_{th j-mb} \leq 15 \text{ K/W}$)
- X. DIODE: multiplier, e.g. varactor, step recovery
- Y. DIODE; rectifying, booster
- Z. DIODE; voltage reference or regulator (transient suppressor diode, with third letter W)

SERIAL NUMBER

Three figures, running from 100 to 999, for devices primarily intended for consumer equipment.*
One letter (Z, Y, X, etc.) and two figures, running from 10 to 99, for devices primarily intended for industrial/professional equipment.*

This letter has no fixed meaning except W, which is used for transient suppressor diodes.

VERSION LETTER

It indicates a minor variant of the basic type either electrically or mechanically. The letter never has a fixed meaning, except letter R, indicating reverse voltage, e.g. collector to case or anode to stud.

SUFFIX

Sub-classification can be used for devices supplied in a wide range of variants called associated types. Following sub-coding suffixes are in use:

1. VOLTAGE REFERENCE and VOLTAGE REGULATOR DIODES: *ONE LETTER and ONE NUMBER*

The LETTER indicates the nominal tolerance of the Zener (regulation, working or reference) voltage

A. 1% (according to IEC 63: series E96)

B. 2% (according to IEC 63: series E48)

C. 5% (according to IEC 63: series E24)

D. 10% (according to IEC 63: series E12)

E. 20% (according to IEC 63: series E6)

The number denotes the typical operating (Zener) voltage related to the nominal current rating for the whole range.

The letter 'V' is used instead of the decimal point.

2. TRANSIENT SUPPRESSOR DIODES: *ONE NUMBER*

The NUMBER indicates the maximum recommended continuous reversed (stand-off) voltage V_R . The letter 'V' is used as above.

3. CONVENTIONAL and CONTROLLED AVALANCHE RECTIFIER DIODES and THYRISTORS: *ONE NUMBER*

The NUMBER indicates the rated maximum repetitive peak reverse voltage (V_{RRM}) or the rated repetitive peak off-state voltage (V_{DRM}), whichever is the lower. Reversed polarity is indicated by letter R, immediately after the number.

4. RADIATION DETECTORS: *ONE NUMBER*, preceded by a hyphen (—)

The NUMBER indicates the depletion layer in μm . The resolution is indicated by a version LETTER.

5. ARRAY OF RADIATION DETECTORS and GENERATORS: *ONE NUMBER*, preceded by a stroke (/).

The NUMBER indicates how many basic devices are assembled into the array.

* When these serial numbers are exhausted the serial number for consumer types may be extended to four figures, and that for industrial types to three figures.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note

This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note

Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note

The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

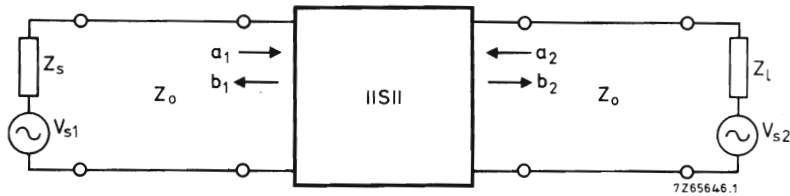
Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

SCATTERING PARAMETERS

In distinction to the conventional h, y and z-parameters, s-parameters relate to traveling wave conditions. The figure below shows a two-port network with the incident and reflected waves a_1 , b_1 , a_2 and b_2 .



$$a_1 = \frac{V_{i1}}{\sqrt{Z_0}}$$

$$a_2 = \frac{V_{i2}}{\sqrt{Z_0}}$$

$$b_1 = \frac{V_{r1}}{\sqrt{Z_0}}$$

$$b_2 = \frac{V_{r2}}{\sqrt{Z_0}}$$

1)

Z_0 = characteristic impedance of the transmission line in which the two-port is connected.

V_i = incident voltage

V_r = reflected (generated) voltage

The four-pole equations for s-parameters are:

$$b_1 = s_{11}a_1 + s_{12}a_2$$

$$b_2 = s_{21}a_1 + s_{22}a_2$$

Using the subscripts i for 11, r for 12, f for 21 and o for 22, it follows that:

$$s_i = s_{11} = \left. \frac{b_1}{a_1} \right|_{a_2 = 0}$$

$$s_r = s_{12} = \left. \frac{b_1}{a_2} \right|_{a_1 = 0}$$

$$s_f = s_{21} = \left. \frac{b_2}{a_1} \right|_{a_2 = 0}$$

$$s_o = s_{22} = \left. \frac{b_2}{a_2} \right|_{a_1 = 0}$$

1) The squares of these quantities have the dimension of power.

S-PARAMETERS

The s-parameters can be named and expressed as follows:

$s_i = s_{11}$ = Input reflection coefficient.

The complex ratio of the reflected wave and the incident wave at the input, under the conditions $Z_1 = Z_0 = 50 \Omega$ and $V_{s2} = 0$.

$s_r = s_{12}$ = Reverse transmission coefficient.

The complex ratio of the generated wave at the input and the incident wave at the output, under the conditions $Z_s = Z_0 = 50 \Omega$ and $V_{s1} = 0$.

$s_f = s_{21}$ = Forward transmission coefficient.

The complex ratio of the generated wave at the output and the incident wave at the input, under the conditions $Z_1 = Z_0 = 50 \Omega$ and $V_{s2} = 0$.

$s_o = s_{22}$ = Output reflection coefficient.

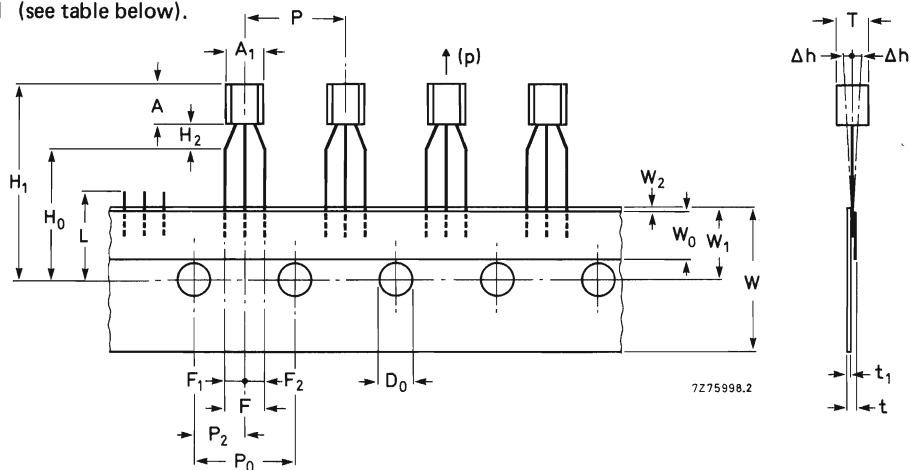
The complex ratio of the reflected wave and the incident wave at the output, under the conditions $Z_s = Z_0 = 50 \Omega$ and $V_{s1} = 0$.

TO-92 VARIANT TRANSISTORS ON TAPE

MECHANICAL DATA

Fig. 1 (see table below).

Dimensions in mm



Item	Symbol	Specifications				Remarks
		min.	nom.	max.	tol.	
Body width	A ₁	4,0		4,8		
Body height	A	4,8		5,2		
Body thickness	T	3,9		4,2		
Pitch of component	P		12,7		± 1	
Feed hole pitch	P ₀		12,7		± 0,3	Cumulative pitch error 1,0 mm/20 pitch
Feed hole centre to component centre	P ₂		6,35		± 0,4	To be measured at bottom of clinch
Distance between outer leads	F		5,08		+ 0,6 - 0,2	
Component alignment	Δh		0	1		At top of body
Tape width	W		18		± 0,5	
Hold-down tape width	W ₀		6		± 0,2	
Hole position	W ₁		9		+ 0,7 - 0,5	
Hold-down tape position	W ₂		0,5		± 0,2	
Lead wire clinch height	H ₀		16		± 0,5	
Component height	H ₁			32,25		
Length of clipped leads	L			11,0		
Feed hole diameter	D ₀		4		± 0,2	
Total tape thickness	t			1,2		t ₁ 0,3-0,6
Lead-to-lead distance	F ₁ , F ₂		2,54		+ 0,4 - 0,1	
Clinch height	H ₂			3		
Pull-out force	(p)	6N				

PACKING

The transistors are supplied on tape in boxes (ammopack) or on reels. The number per reel is 1600 and per ammobox 2000*.

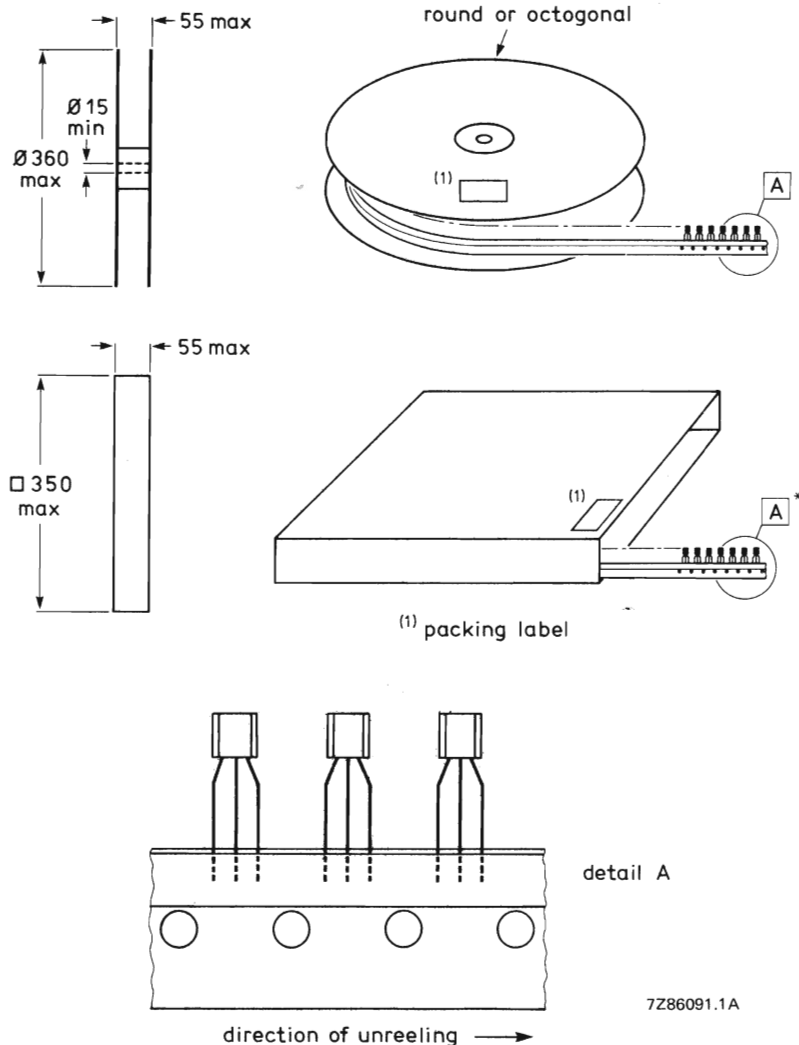


Fig. 2 Dimensions (in mm) of reel and box.

DROPOUTS

A maximum of 0,5% of the specified number of transistors in each packing may be missing. Up to 3 consecutive components may be missing provided the gap is followed by 6 consecutive components.

TAPE SPLICING

Slice the carrier tape on the back and/or front so that the feed hole pitch (P_0) is maintained (see Fig. 3).

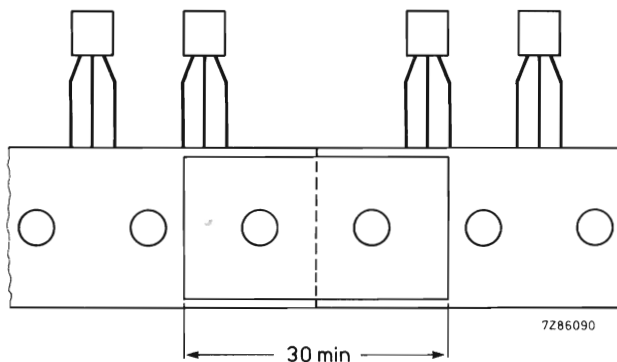


Fig. 3 Jointing tape with splicing patch.

- * The ammobox has 80 layers of 25 transistors each.
Each layer contains 25 transistors plus one empty position in order to fold the layer correctly.
The ammobox is accessible from both sides enabling the user to choose between "normal" (see Fig. 2) and "reverse" tape.

TAPE AND REEL SPECIFICATION

Semiconductors in SOT-23, SOT-143 and SOT-89 encapsulations can be delivered in reel packing for automatic placement on hybrid circuits and printed circuit boards. The devices are placed with the mounting side downwards in compartments.

A separate reel packing for SOT-89 encapsulation is given in Fig. 3.

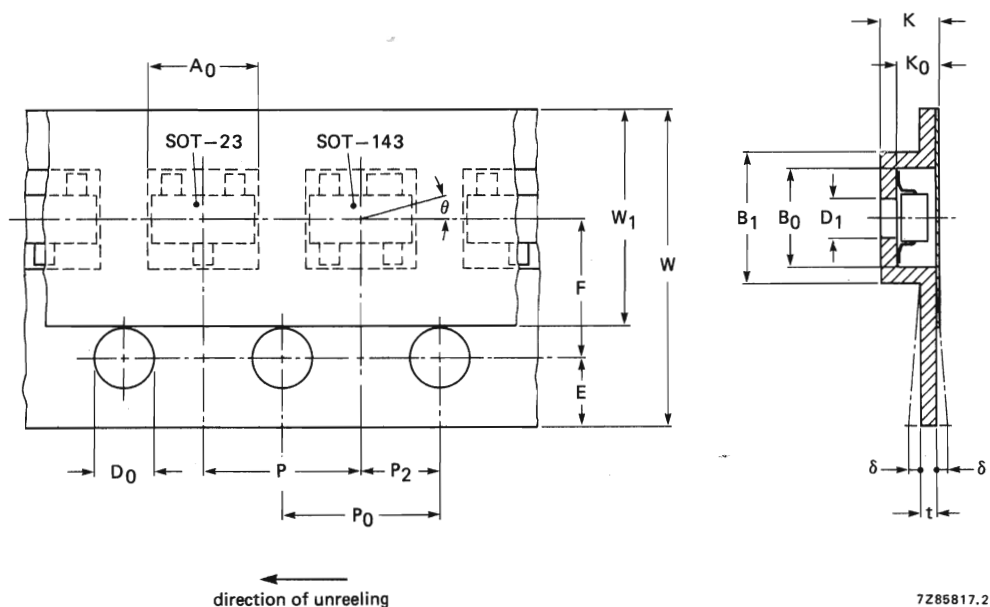
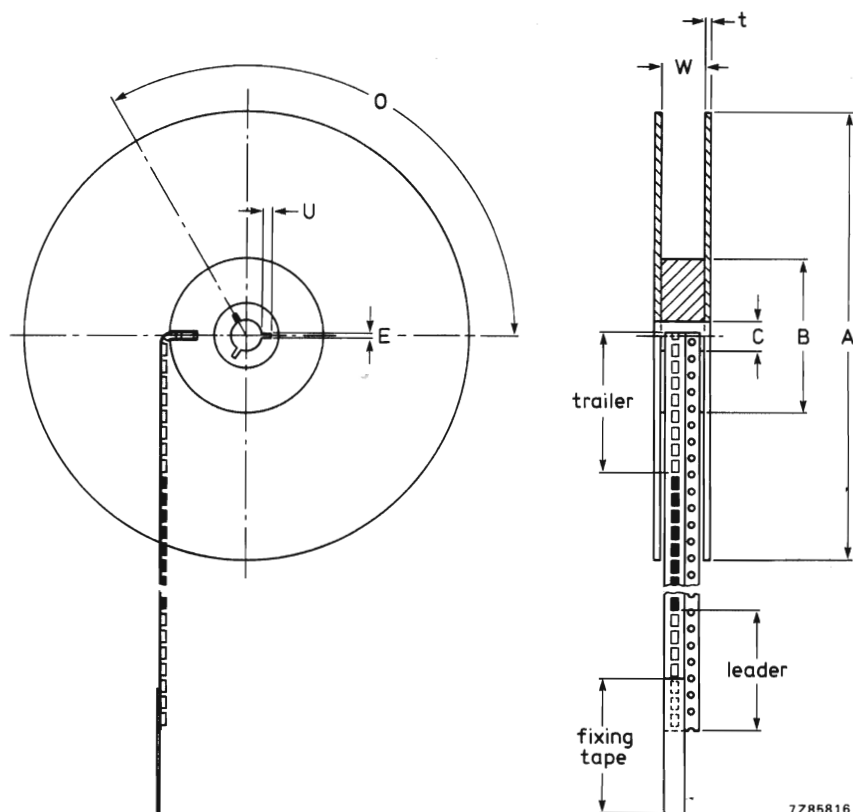


Fig. 1 Configuration of bandolier. Dimensions in mm.

Compartment			tol.			Centre line dimensions			tol.		
length	A ₀	component length			+0,2	length direction	P ₂	2,0			± 0,05
width	B ₀	component width			+0,2	width direction	F	3,5			± 0,05
depth	K ₀		0,95		+0,2	Fixing tape					
width outside	B ₁		3,3		max.	width	W ₁	5,5			± 0,25
pitch	P		4,0		± 0,1	thickness	—	0,1			max.
deviation	Θ		15°		max.	Carrier tape					
hole diameter	D ₁		1		min.	width	W	8,0			± 0,2
Sprocket hole						bending	δ	0,3			max.
diameter	D ₀		1,5		+0,1	thickness	t	0,4			max.
pitch	P ₀		4,0		± 0,1	Overall thickness					
distance	E		1,75		± 0,1		K	1,5			max.
cumulative (10)											
pitch error					± 0,1						



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Fig. 2 Configuration of reel and flange (dimensions in mm).

Flange			tol.
diameter	A	180	+0 -2
thickness	t	1,5	+0,5 -0,1
space between flanges	W	9,5	± 0,5

Hub			tol.
diameter	B	62	± 1,5
spindle hole	C	12,75	+0,15 -0
key slit			
width	E	2	± 0,5
depth	U	4	± 0,5
location	O	120	degrees

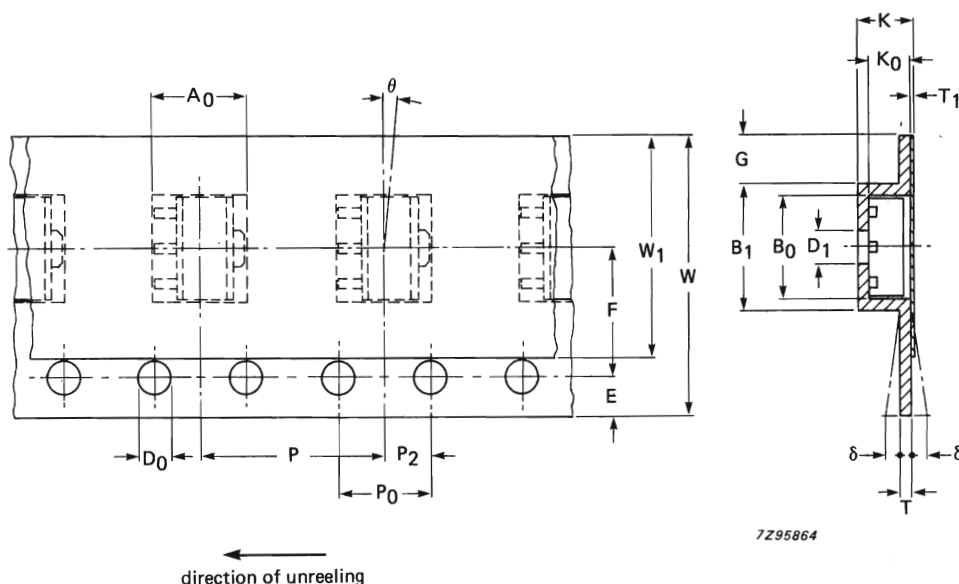
Amount of devices per reel

The bandolier of a 180 mm reel contains at least 3000 devices with no more than 15 empty compartments (0,5%). Three consecutive empty places might be found provided this gap is followed by 6 consecutive devices.

The carrier tape (leader) starts with at least 75 empty positions (equivalent to 300 mm); the covering foil is at least 300 mm. In order to fix the carrier tape a self-adhesive tape of 20 to 50 mm is applied.

At the end of the bandolier (trailer) at least 75 empty positions (equivalent to a length of 300 mm) and 300 mm foil. For fixing onto the reel a self-adhesive tape of 20 to 50 mm is applied.

Semiconductors in SOT-89 encapsulations can also be delivered in reel packing for automatic placement on hybrid circuits and printed circuit boards. The devices are placed with the mounting side downwards in compartments. Total number of devices per reel is 1000.



7Z95864

Fig. 3 Configuration of bandolier. Dimensions in mm.

Compartment			tol.			Centre line dimensions			tol.		
length	A ₀	component length				length direction	P ₂	2,0		± 0,05	
width	B ₀	component width				width direction	F	5,5		± 0,1	
depth	K ₀	component depth				Fixing tape					
width outside	B ₁	5,7		max.		width	W ₁	9,5		max.	
pitch	P	8,0		± 0,1		thickness	T ₁	0,1		max.	
deviation	θ	± 5°		max.		Carrier tape					
hole diam.	D ₁	1,5		min.		width	W	12		± 0,2	
Sprocket hole						bending	δ	0,3		max.	
diameter	D ₀	1,5		+ 0,1		thickness	T	0,4		max.	
pitch	P ₀	4,0		± 0,1		Overall thickness					
distance	E	1,75		± 0,1		distance	K	2,4		max.	
cumulative (10)							G	1,8		min.	
pitch error				± 0,1							

SOLDERING RECOMMENDATIONS

SOT-23, SOT-143 AND SOT-89 ENVELOPES

SOT-23, SOT-143 and SOT-89 devices are ideally suited for placement onto thick and thin film substrates and printed circuit boards.

To assure reliable and consistent connections particular attention should be paid to:

1. Flux

A non-active flux is recommended. Where active fluxes are employed, great care in subsequent substrate cleaning must be exercised.

2. Metal-alloy solder or solder paste

Correct choice of solder alloy or solder paste to be employed e.g. 62% Sn, 36% Pb, 2% Ag or 60% Sn/40% Pb. Any paste used should contain at least 85% metal dry weight.

3. Soldering temperature

This will vary according to the actual method employed.

REFLOW SOLDERING

The preferred technique for mounting microminiature components on hybrid thick and thin-film is the method of reflow soldering.

The tags of SOT-23, SOT-143 and SOT-89 envelopes are pre-tinned and the best results are obtained if a similar solder is applied to the corresponding soldering areas on the substrate. This can be done by either dipping the substrate in a solder bath or by screen printing a solder paste.

The maximum temperature of the leads or tab during the soldering cycle should not exceed 285 °C. The most economic method of soldering is a process in which all different components are soldered simultaneously for example SOT-23, SOT-143 or SOT-89 devices, capacitors and resistors.

Having first been fluxed, all components are positioned on the substrate. The slight adhesive force of the flux is sufficient to keep the components in place. Solder paste contains a flux and has therefore good inherent adhesive properties which eases positioning of the components.

With the components in position the substrate is heated to a point where the solder begins to flow. This can be done on a heating plate or on a conveyor belt running through an infrared tunnel. The maximum allowed temperature of the plastic body of a device must be kept below 280 °C during the soldering cycle. For further temperature behaviour during the soldering process see Figs 2 and 3.

The surface tension of the liquid solder tends to draw the tags of the device towards the centre of the soldering area and has thus a correcting effect on slight mispositionings. However, if the layout leaves something to be desired the same effect can result in undesirable shifts; particularly if the soldering areas on the substrate and the components are not concentrically arranged. This problem can be solved using a standard contact pattern, which leaves sufficient scope for the self-positioning effect (see Figs 4 and 5).

After cooling the connections may be visually inspected and, where necessary, repaired with a light soldering iron. Finally any remaining flux must be removed carefully.

WAVE SOLDERING

The normal (dual) wave soldering process can also be applied to SOT-23 and SOT-143 envelopes. We do not recommend SOT-89 for wave soldering.

IMMERSION SOLDERING

Where a complete substrate or printed circuit board is immersed in solder:

- The temperature of the soldering bath should not exceed 280 °C.
- The duration of the soldering cycle should not exceed 10 seconds.
- Forced cooling may be applied (see Fig. 1).

HAND SOLDERING

It is possible to solder microminiature devices with a light hand-held soldering iron, but this method has obvious drawbacks and should therefore be restricted to laboratory use and/or incidental repairs on production circuits.

- It is time-consuming and expensive.
- The device cannot be positioned accurately and therefore the connecting tags may come into contact with the substrate and damage it.
- There is a great risk of breaking either substrate or even internal connections inside the encapsulation.
- The envelope may be damaged by the iron.

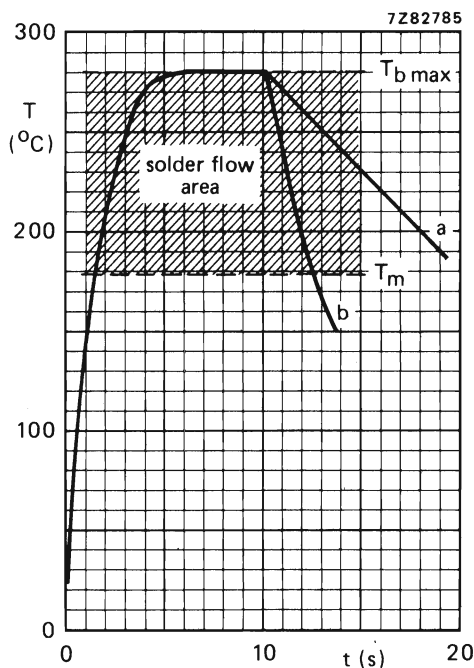


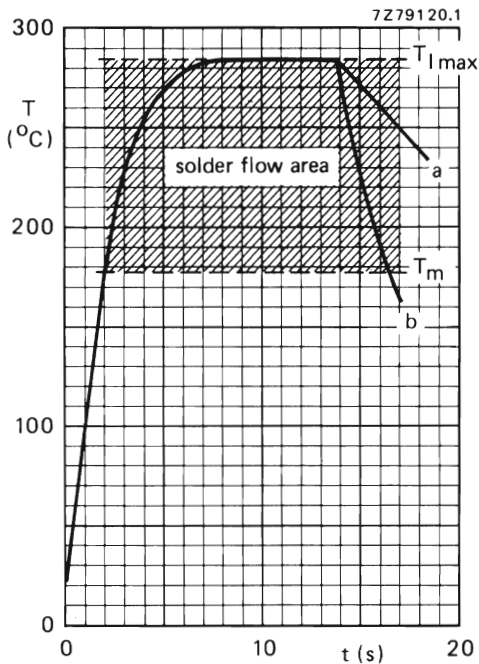
Fig. 1 Device temperature during *immersion* soldering.

Maximum time of immersion in soldering bath is 10 seconds at an ambient temperature of 25 °C.

a = free convection cooling; b = forced cooling.

$T_{b \text{ max}}$ = maximum bath temperature (280 °C).

T_m = melting temperature of solder (179 °C).



a = free convection cooling.

b = permissible forced cooling.

$T_{l\max}$ = Maximum lead or tab temperature = 285 °C.

T_m = Melting point of the solder is 179 °C.

T_{amb} = 25 °C.

Time of heat supply:

without preheating max. 14 s

with preheating max. 10 s

Maximum time of preheating 45 s

Fig. 2 Reflow soldering without preheating.

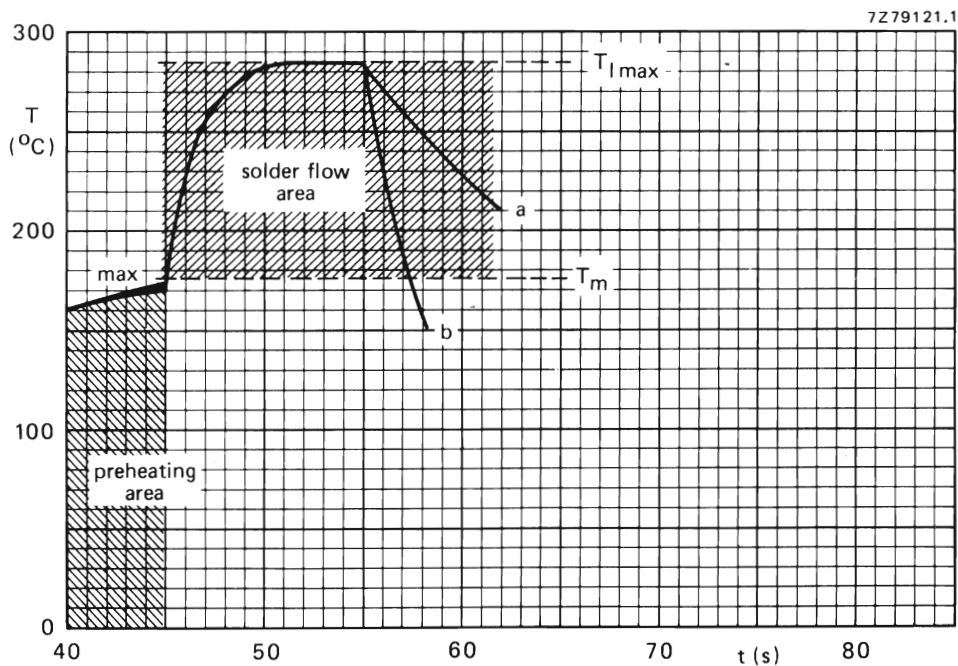


Fig. 3 Reflow soldering with preheating.

Minimum required dimensions of metal connection pads on hybrid thick and thin-film substrates.

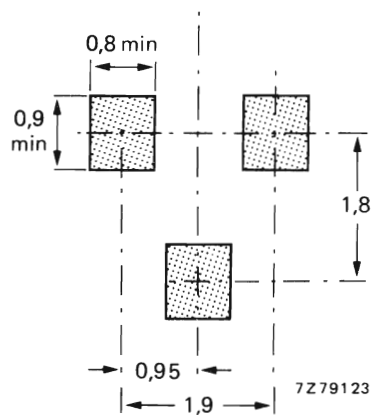


Fig. 4 SOT-23 pattern.

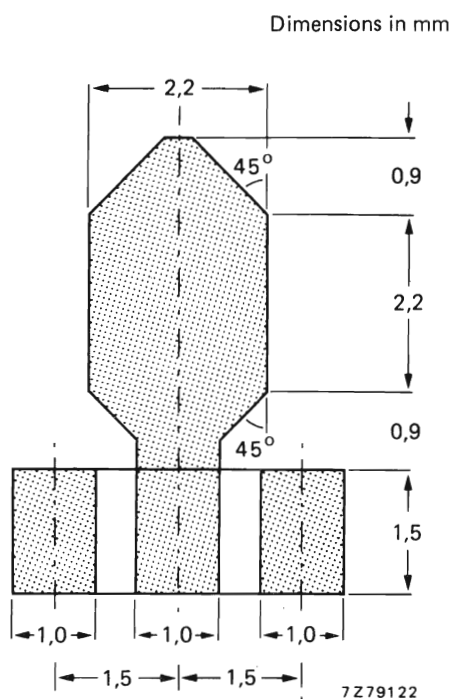


Fig. 5 SOT-89 pattern.

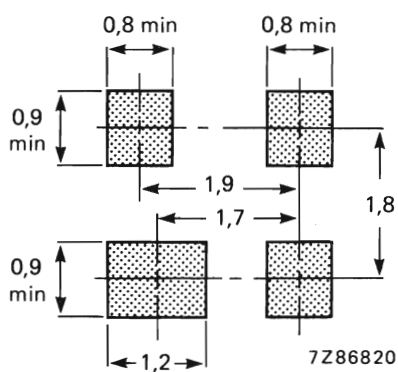


Fig. 6 SOT-143 pattern.

SOLDERING RECOMMENDATIONS SOT-103

Transistors in SOT-103 envelopes may be mounted with leads flat (Fig. 1) or bent (Figs 2 and 3). Different soldering procedures apply for the different styles of mounting.

FLAT-LEAD MOUNTING

Soldering by hand

Avoid putting any force on the leads during or just after soldering.

Solder the four leads one at a time, *not* simultaneously.

Proceed from one lead to the adjacent lead, *not* to the opposite one.

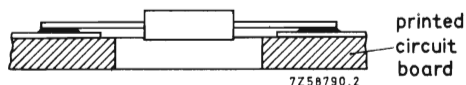


Fig. 1

Solder temperature	max.	300 °C
Soldering time	max.	5 s
Solder-to-case distance	min.	2 mm

BENT-LEAD MOUNTING

If leads are bent, all four may be soldered simultaneously if desired.

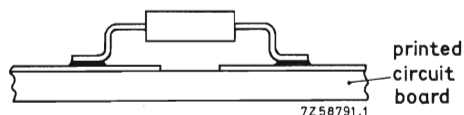


Fig. 2

Solder temperature	max.	300 °C
Soldering time	max.	10 s

DIP OR WAVE SOLDERING

When dip or wave soldering, the maximum allowable temperature of the solder is 260 °C. This temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the lead projections, but the temperature of the body must not exceed the specified storage maximum.

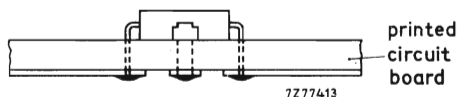


Fig. 3

Solder temperature	max.	260 °C
Soldering time	max.	5 s

THERMAL CHARACTERISTICS OF SOT-23 AND SOT-143 ENVELOPES

The heat generated in a semiconductor chip normally flows by various paths to the surroundings (ambient).

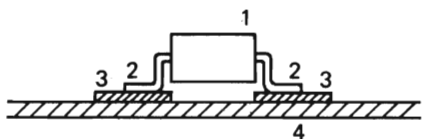
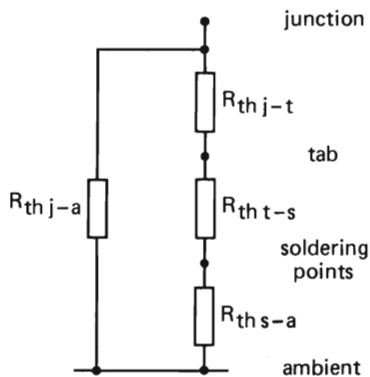


Fig. 1.

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1. Heat radiation from the envelope to ambient (1).
This heat transfer can be neglected when the envelope is mounted on a substrate or printed circuit board.
2. Heat transmission via leads (2) soldering points (3) and substrate (4).



7Z89073

Fig. 2 Thermal behaviour of heat flow when the device is mounted on a substrate or printed circuit board.

- $R_{th\ j-t}$ = Thermal resistance from junction to tab.
 $R_{th\ t-s}$ = Thermal resistance from tab to soldering points.
 $R_{th\ s-a}$ = Thermal resistance from soldering points to ambient.
 $R_{th\ j-a}$ = Thermal resistance from junction to ambient.

Heat transfer directly from envelope to ambient

This depends on the difference between the temperatures of envelope and the surroundings. When the device is mounted on a substrate or printed circuit board direct heat flow can usually be neglected in relation to the heat flow via leads and substrate.

Thus the thermal model can be as in Fig. 3.

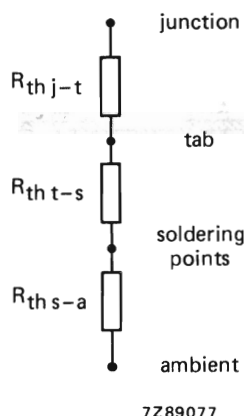


Fig. 3 Basic thermal model.

Heat transfer from junction to tab

This is an internal heat transfer and has been measured. In general it is:

for high-frequency transistors, low-power diodes and (MOS) FETs	60 K/W
for low-frequency and switching transistors	50 K/W
for low-frequency medium-power transistors	30 K/W

Heat transfer from tab to soldering points

This value has also been measured for SOT-23 with $P_{tot} < 350$ mW	280 K/W
for types of semiconductors in this envelope with $P_{tot} < 425$ mW	260 K/W
for types of semiconductors in a SOT-143 envelope this value is	310 K/W

Heat transfer from soldering points to ambient

This depends on the shape and material of tracks and substrate. In figures 4 and 5 standard mounting conditions are given to set up the maximum power ratings for SOT-23 and SOT-143 encapsulations.

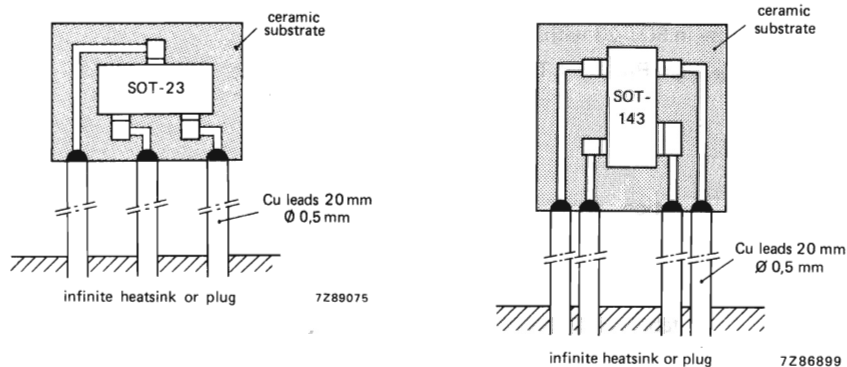


Fig. 4 Test circuits SOT-23 and SOT-143 mounting conditions on a ceramic substrate.

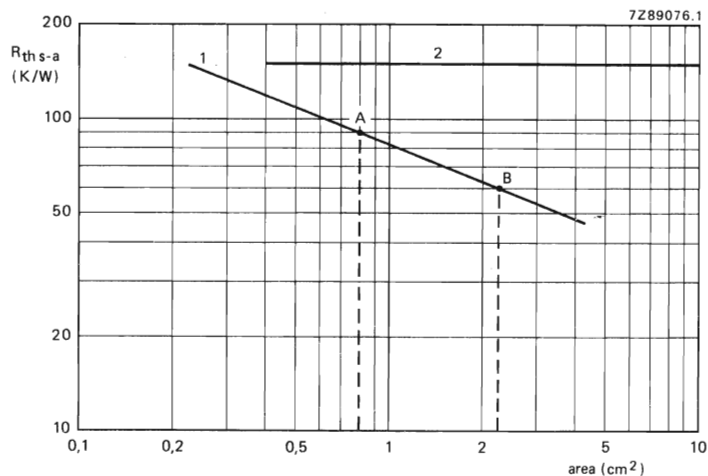


Fig. 5 Heat transfer from soldering points to ambient.

1. Ceramic substrate

Point A on the curve in Fig. 5 is for an area of the ceramic substrate of 8 mm x 10 mm x 0,7 mm for the maximum rating of all high-frequency, low-frequency and switching transistors and also for all diodes.

Point B on the curve in Fig. 5 is for an area of the ceramic substrate of 15 mm x 15 mm x 0,7 mm for the maximum rating of low-frequency medium-power semiconductors.

2. Printed circuit board

$R_{th\ s-a} = 150$ K/W for SOT-23 and SOT-143 envelopes mounted on a printed circuit board.

The values for the thermal resistance from junction to tab, and tab to soldering points, are mentioned on page 2 and Fig. 5.

The formula for devices in SOT-23 with one crystal can be generalized:

$$T_j = P (R_{th\ j-t} + R_{th\ t-s} + R_{th\ s-a}) + T_{amb}$$

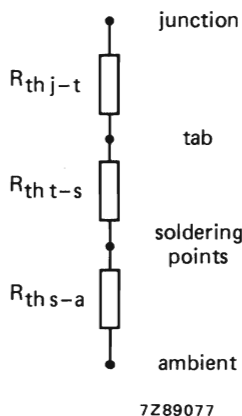


Fig. 6 Thermal model of SOT-23 envelopes with one crystal.

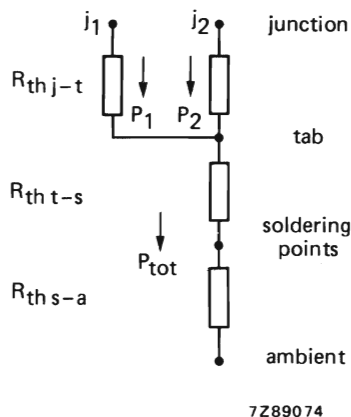


Fig. 7 Thermal model of SOT-23 envelopes with two crystals (double diode).

The formulae for devices with two crystals (double diodes) are:

$$T_{tab} = P_{tot} \cdot (R_{th\ t-s} + R_{th\ s-a}) + T_{amb} = P_{tot} (280 + 90) + T_{amb}$$

$$T_{j1} = (P_1 \times R_{th\ j-t}) + T_{tab} = P_1 \cdot 60 + T_{tab}$$

$$T_{j2} = (P_2 \times R_{th\ j-t}) + T_{tab} = P_2 \cdot 60 + T_{tab}$$

As mentioned on page 2:

$R_{th\ j-t}$ for diodes is 60 K/W.

$R_{th\ s-a}$ (area 8 mm x 10 mm x 0,7 mm) = 90 K/W.

$R_{th\ t-s}$ for all semiconductors in SOT-23 = 280 K/W.

Thus:

$$T_{j1} = 60 P_1 + 370 P_{tot} + T_{amb}$$

$$T_{j2} = 60 P_2 + 370 P_{tot} + T_{amb}$$

DEVICE DATA

J-FETS

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for hi-fi amplifiers and other audio-frequency equipment.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}		2 to 12 mA
Transfer admittance (common source) $V_{DS} = 15\text{ V}; V_{GS} = 0; f = 1\text{ kHz}$	$ Y_{fs} $	typ.	3,5 mS
Noise figure at $V_{DS} = 15\text{ V}; V_{GS} = 0$ $f = 1\text{ kHz}; R_G = 1\text{ M}\Omega$	F	<	2 dB

MECHANICAL DATA

Dimensions in mm

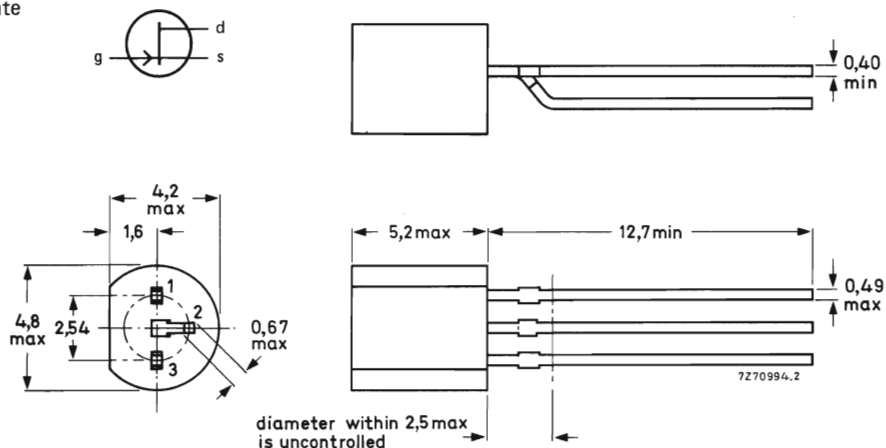
Fig. 1 TO-92 variant.

Pinning:

1 = drain

2 = source

3 = gate



Note: Drain and source are interchangeable

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Gate current	I_G	max.	10	mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300	mW
Storage temperature	T_{stg}	-65 to +150		$^{\circ}\text{C}$
Junction temperature	T_j	max.	150	$^{\circ}\text{C}$

THERMAL RESISTANCE

→ From junction to ambient in free air	$R_{th\ j-a}$	=	420	K/W
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CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off current

$-V_{GS} = 20\text{ V}; V_{DS} = 0$

 $-I_{GSS}$

BC264A	B	C	D
< 10	10	10	10

nA

Drain current ¹⁾

$V_{DS} = 15\text{ V}; V_{GS} = 0$

 I_{DSS}

> 2,0	3,5	5,0	7,0
< 4,5	6,5	8,0	12,0

mA

mA

Gate-source breakdown voltage

$-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$

 $-V_{(BR)GSS}$

> 30	30	30	30
------	----	----	----

V

Gate-source voltage

$I_D = 200\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$

 $-V_{GS}$

> 0,4	0,4	0,4	0,4
-------	-----	-----	-----

V

$I_D = 1,0\text{ mA}; V_{DS} = 15\text{ V}$

 $-V_{GS}$

> 0,2	—	—	—
< 1,2	—	—	—

V

V

$I_D = 1,5\text{ mA}; V_{DS} = 15\text{ V}$

 $-V_{GS}$

> —	0,4	—	—
< —	1,4	—	—

V

V

$I_D = 2,5\text{ mA}; V_{DS} = 15\text{ V}$

 $-V_{GS}$

> —	—	0,5	—
< —	—	1,5	—

V

V

$I_D = 3,5\text{ mA}; V_{DS} = 15\text{ V}$

 $-V_{GS}$

> —	—	—	0,6
< —	—	—	1,6

V

V

Gate-source cut-off voltage

$I_D = 10\text{ nA}; V_{DS} = 15\text{ V}$

 $-V_{(P)GS}$

> 0,5	0,5	0,5	0,5
-------	-----	-----	-----

V

y-parameters at $T_{amb} = 25\text{ }^{\circ}\text{C}$

$V_{DS} = 15\text{ V}; V_{GS} = 0; f = 1\text{ kHz}$

Transfer admittance

 $|y_{fs}|$

> 2,5	3,0	3,5	4,0
-------	-----	-----	-----

mS

$V_{DS} = 15\text{ V}; -V_{GS} = 1\text{ V}; f = 1\text{ MHz}$

Input capacitance

 C_{is}

typ. 4,0 pF

Feedback capacitance

 C_{rs}

typ. 1,2 pF

Output capacitance

 C_{os}

typ. 1,6 pF

Noise figure at $f = 1\text{ kHz}; R_G = 1\text{ M}\Omega$

$V_{DS} = 15\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^{\circ}\text{C}$

F

typ. 0,5 dB
< 2 dBEquivalent noise voltage at $T_{amb} = 25\text{ }^{\circ}\text{C}$

$V_{DS} = 15\text{ V}; V_{GS} = 0; f = 10\text{ Hz}$

 V_n/\sqrt{B} typ. 40 nV/ $\sqrt{\text{Hz}}$ ¹⁾ Measured under pulse conditions.

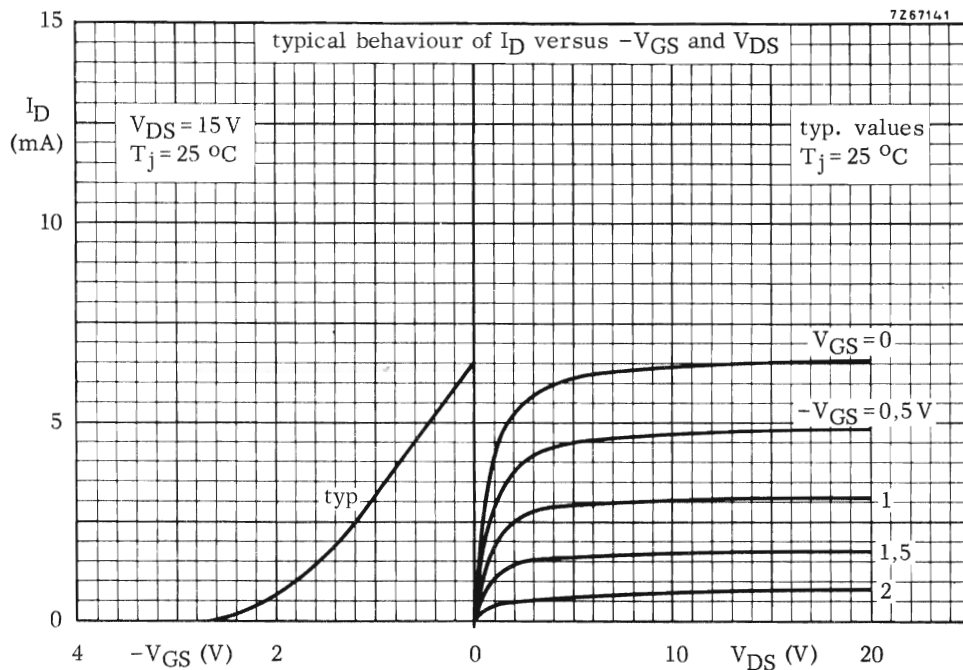


Fig. 2

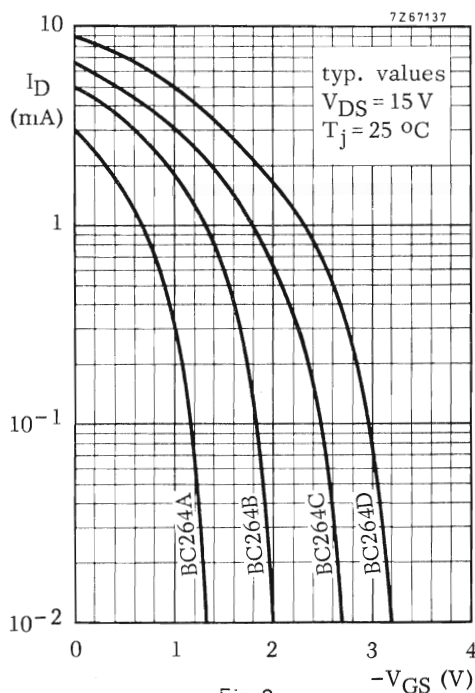


Fig. 3

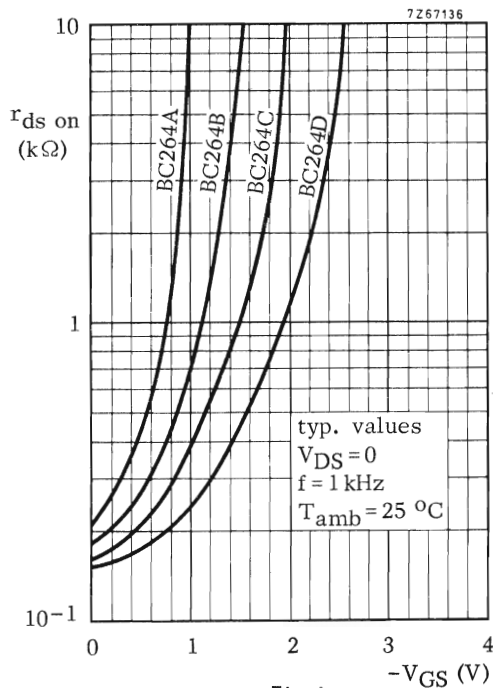


Fig. 4

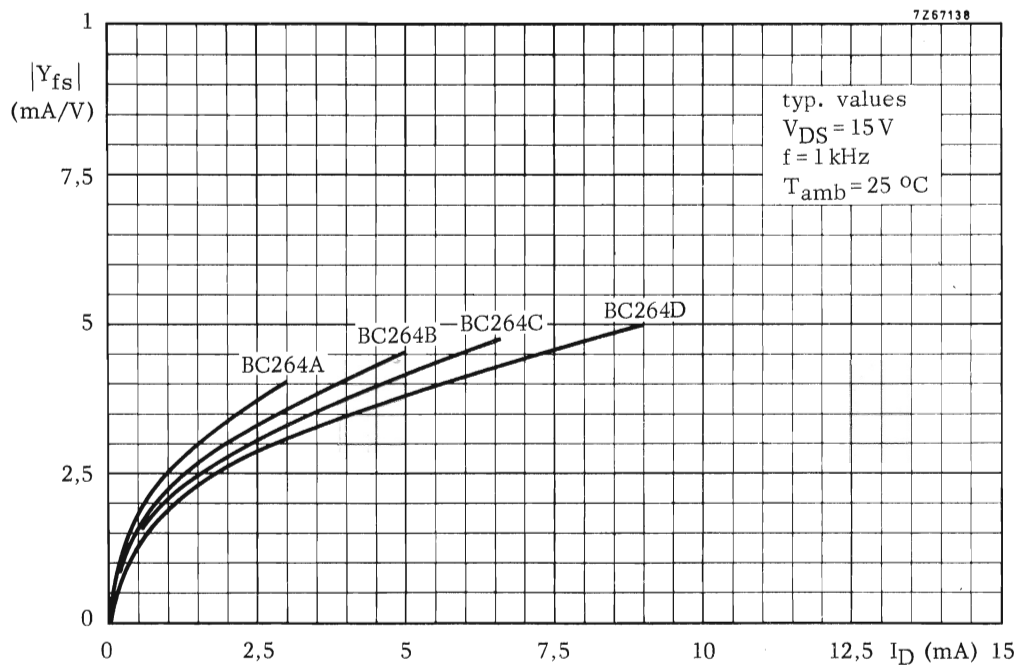


Fig. 5

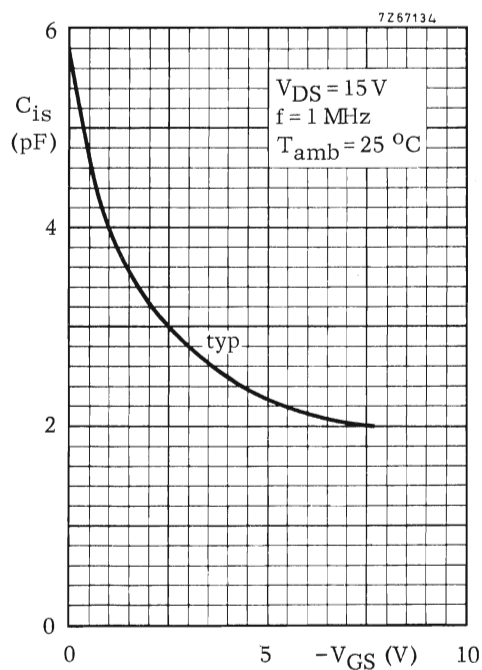


Fig. 6

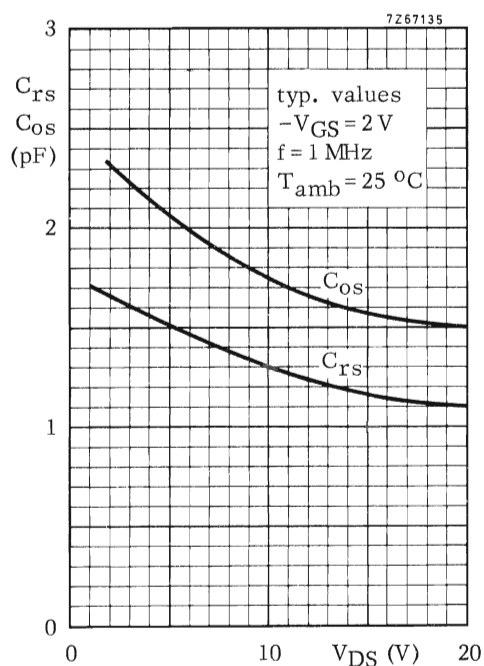


Fig. 7

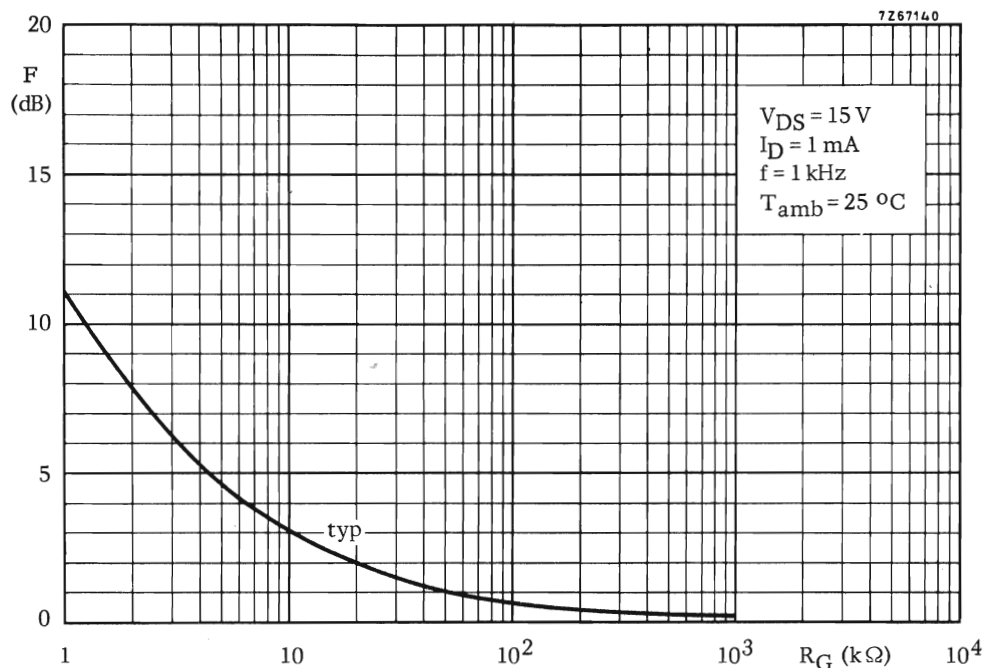


Fig. 8

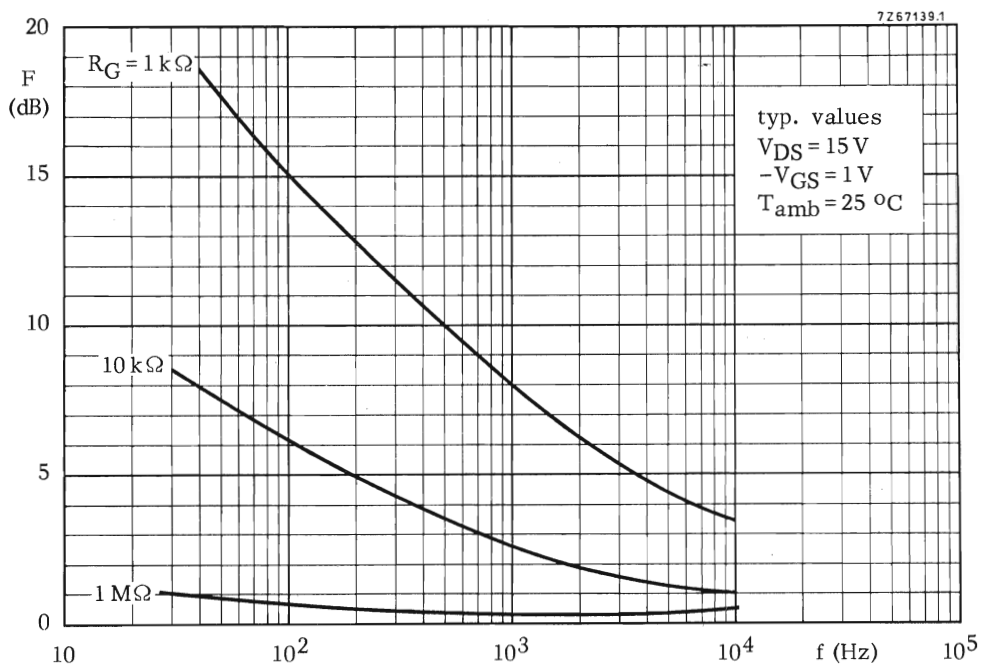


Fig. 9

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

General purpose symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications in l.f. and d.c. amplifiers, and in h.f. amplifiers.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30 V		
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V		
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW		
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}	BF245A/0	A	B	C
	$>$	0,5	2,0	6	12 mA
	$<$	2,1	6,5	15	25 mA
Gate-source cut-off voltage $I_D = 10\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	0,25 to 8,0 V			
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 20\text{ V}; -V_{GS} = 1\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	C_{rs}	typ.	1,1 pF		
Transfer admittance (common source) $V_{DS} = 15\text{ V}; V_{GS} = 0; f = 1\text{ kHz}; T_{amb} = 25\text{ }^{\circ}\text{C}$	$ Y_{fs} $	3,0 to 6,5 mS			

MECHANICAL DATA

Dimensions in mm

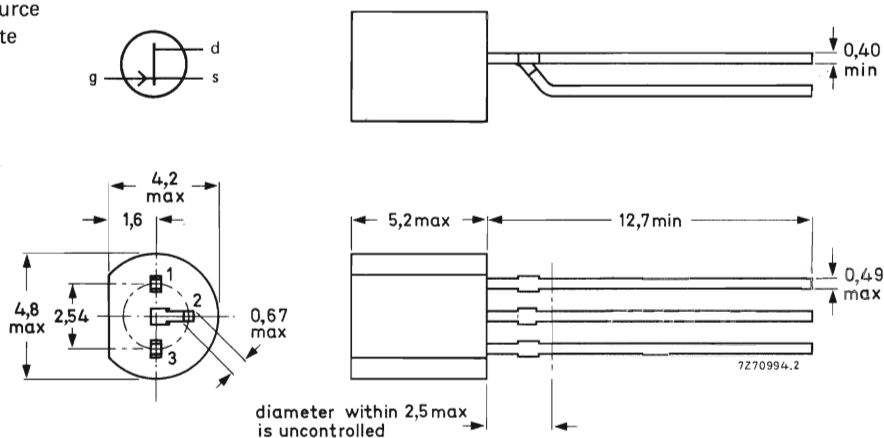
Fig. 1 TO-92 variant.

Pinning:

1 = drain

2 = source

3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	I_D	max.	25 mA
Gate current	I_G	max.	10 mA
Power dissipation			
up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
up to $T_{amb} = 90\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW 1)
Storage temperature	T_{stg}		$-65\text{ to }+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	0,25 K/mW
From junction to ambient	$R_{th\ j-a}$	=	0,20 K/mW 1)

CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

		BF245A	B	C
Gate cut-off current				
$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	< 5	5	5 nA
$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_j = 125\text{ }^{\circ}\text{C}$	$-I_{GSS}$	$< 0,5$	0,5	0,5 μA
Drain current 2)				
$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS\ 3)}$	> 2 $< 6,5$	6,0 15,0	12 mA 25 mA
Gate-source breakdown voltage				
$-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	> 30	30	30 V
Gate-source voltage				
$I_D = 200\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS\ 3)}$	$> 0,4$ $< 2,2$	1,6 3,8	3,2 V 7,5 V

1) Transistor mounted on printed circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: $t_p = 300\text{ }\mu\text{s}; \delta \leq 0,02$.

3) BF245A/0: $I_{DSS} = 0,5\text{ to }2,1\text{ mA}; -V_{GS} = 0,2\text{ to }1,0\text{ V}$
 BF245A/1: $I_{DSS} = 1,9\text{ to }3,0\text{ mA}; -V_{GS} = 0,4\text{ to }1,0\text{ V}$
 BF245A/2: $I_{DSS} = 3,0\text{ to }4,5\text{ mA}; -V_{GS} = 0,7\text{ to }1,4\text{ V}$
 BF245A/3: $I_{DSS} = 4,5\text{ to }6,5\text{ mA}; -V_{GS} = 1,1\text{ to }2,2\text{ V}$.

Gate-source cut-off voltage

$$I_D = 10 \text{ nA}; V_{DS} = 15 \text{ V}$$

y-parameters at $T_{amb} = 25^\circ\text{C}$ (common source)

$$V_{DS} = 15 \text{ V}; V_{GS} = 0$$

$$f = 1 \text{ kHz}$$

Transfer admittance

Output admittance

$$f = 200 \text{ MHz}$$

Input conductance

Reverse transfer admittance

Transfer admittance

Output conductance

$$V_{DS} = 20 \text{ V}; -V_{GS} = 1 \text{ V}$$

$$f = 1 \text{ MHz}$$

Input capacitance

Feedback capacitance

Output capacitance

Cut-off frequency *

$$V_{DS} = 15 \text{ V}; V_{GS} = 0$$

Noise figure at $f = 100 \text{ MHz}$; $R_G = 1 \text{ k}\Omega$ (common source)

$$V_{DS} = 15 \text{ V}; V_{GS} = 0; T_{amb} = 25^\circ\text{C}$$

input tuned to minimum noise

$$-V_{(P)GS} \quad 0,25 \text{ to } 8,0 \text{ V}$$

$$|y_{fs}| \quad 3,0 \text{ to } 6,5 \text{ mS}$$

$$|y_{os}| \quad \text{typ. } 25 \text{ }\mu\text{S}$$

$$g_{is} \quad \text{typ. } 250 \text{ }\mu\text{S}$$

$$|y_{rs}| \quad \text{typ. } 1,4 \text{ mS}$$

$$|y_{fs}| \quad \text{typ. } 6 \text{ mS}$$

$$g_{os} \quad \text{typ. } 40 \text{ }\mu\text{S}$$

$$C_{is} \quad \text{typ. } 4,0 \text{ pF}$$

$$C_{rs} \quad \text{typ. } 1,1 \text{ pF}$$

$$C_{os} \quad \text{typ. } 1,6 \text{ pF}$$

$$f_{gfs} \quad \text{typ. } 700 \text{ MHz}$$

$$F \quad \text{typ. } 1,5 \text{ dB}$$

* The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

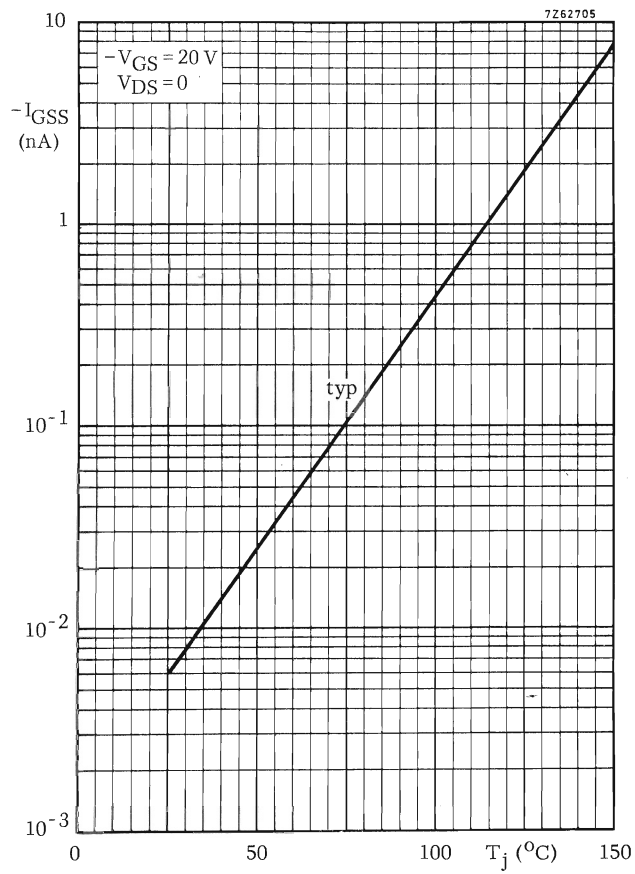


Fig. 2

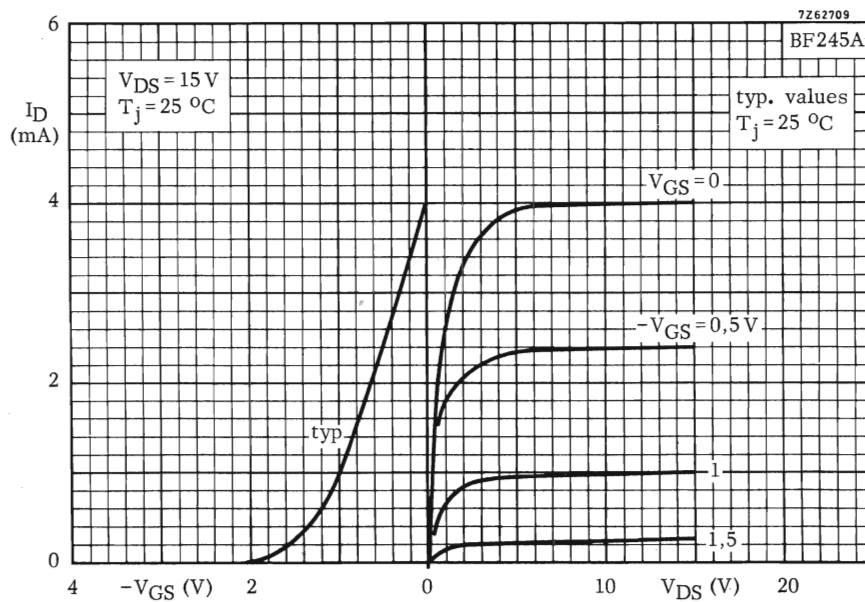


Fig. 3

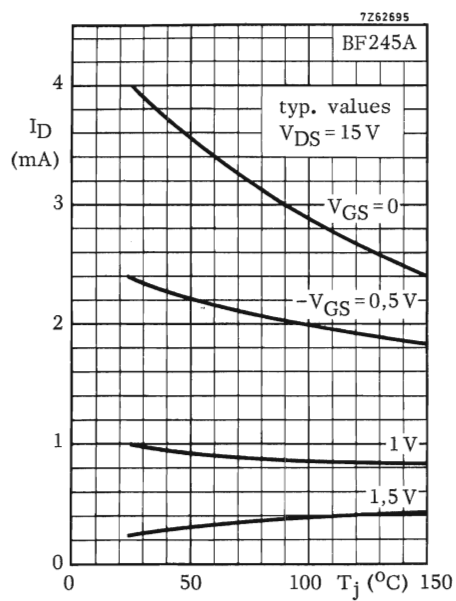


Fig. 4

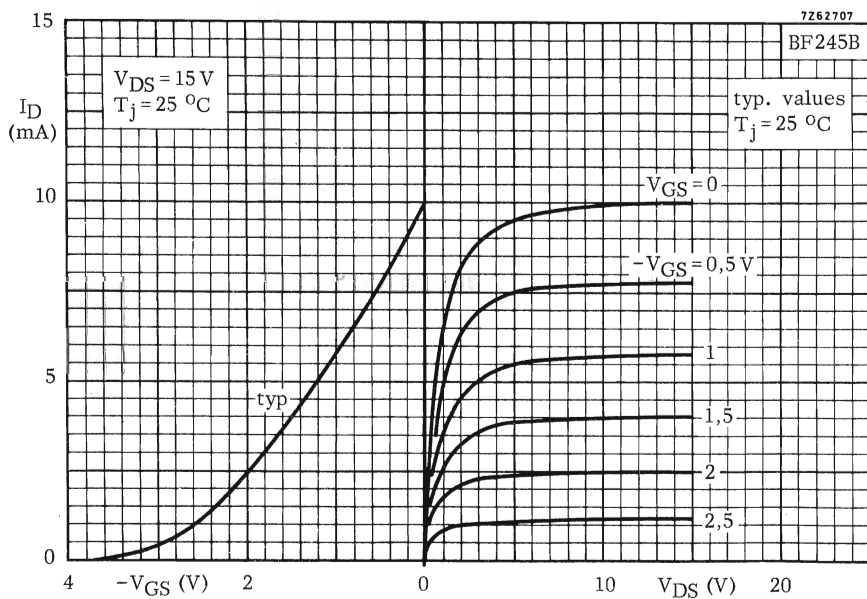


Fig. 5

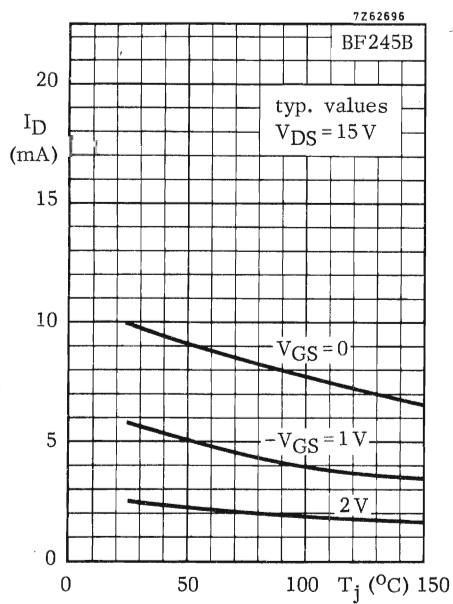
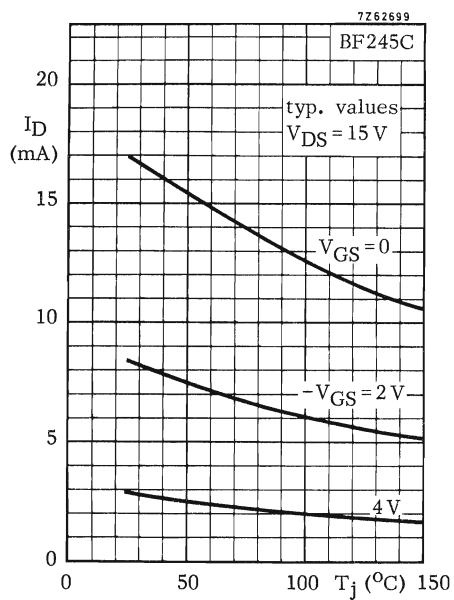
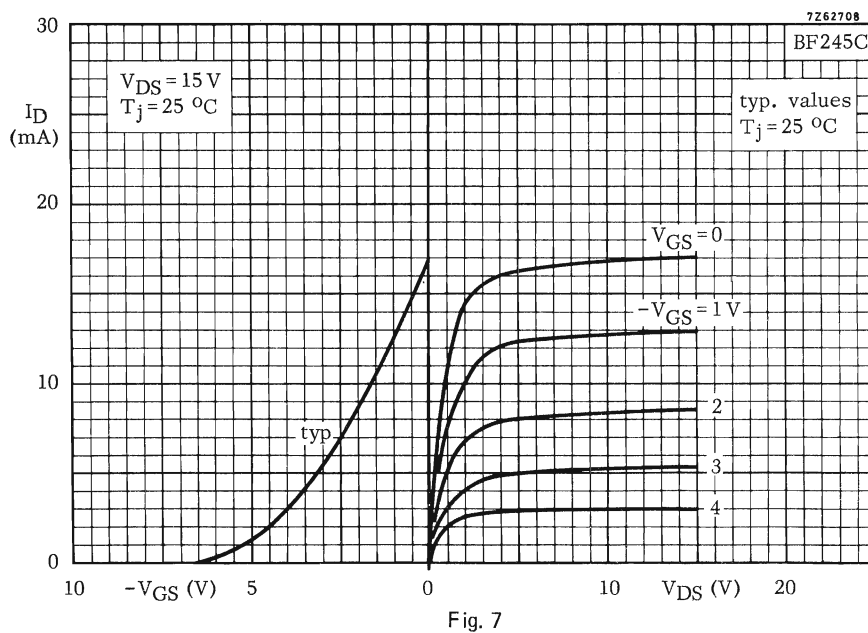


Fig. 6



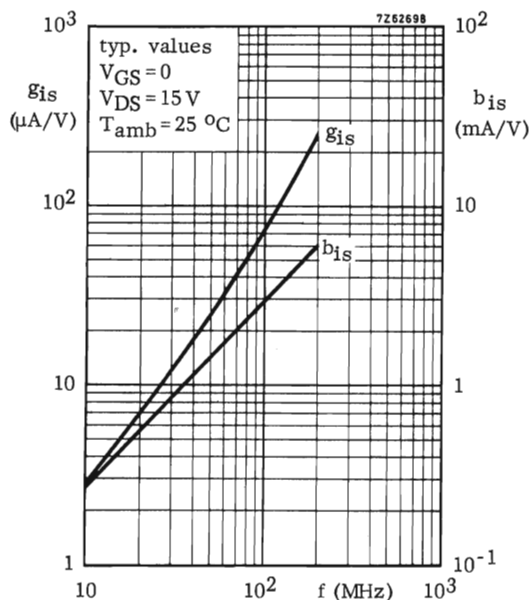


Fig. 9

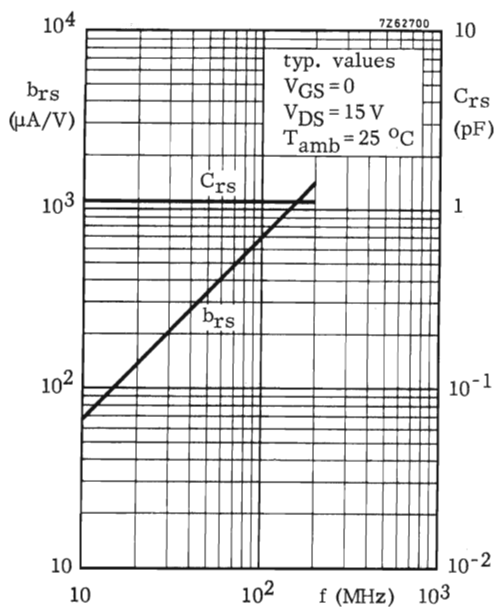


Fig. 10

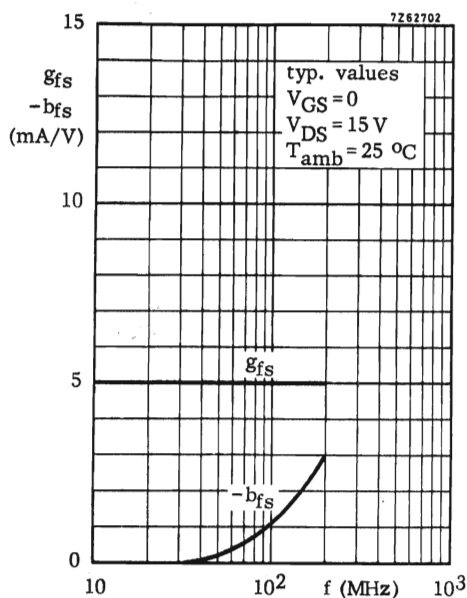


Fig. 11

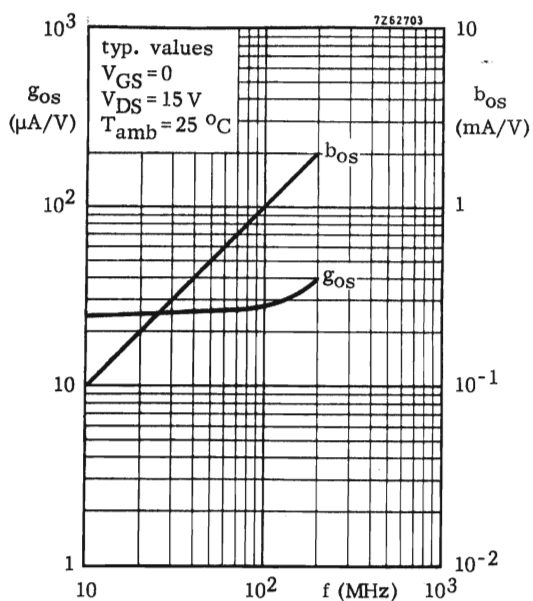


Fig. 12

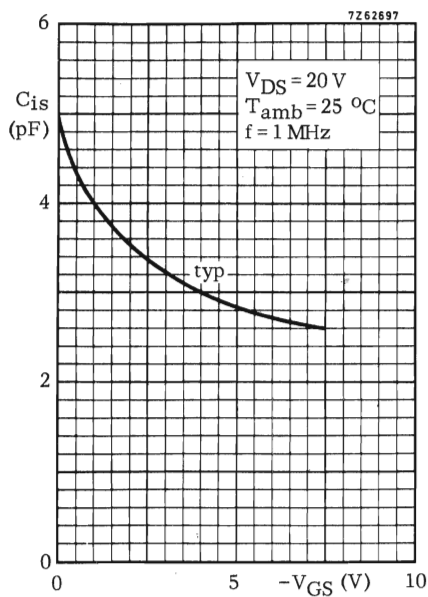


Fig. 13

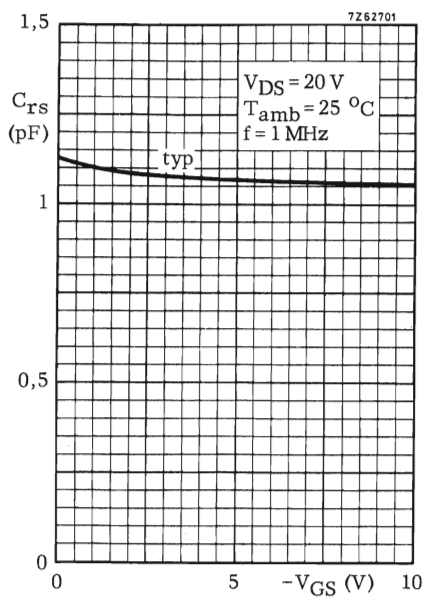


Fig. 14

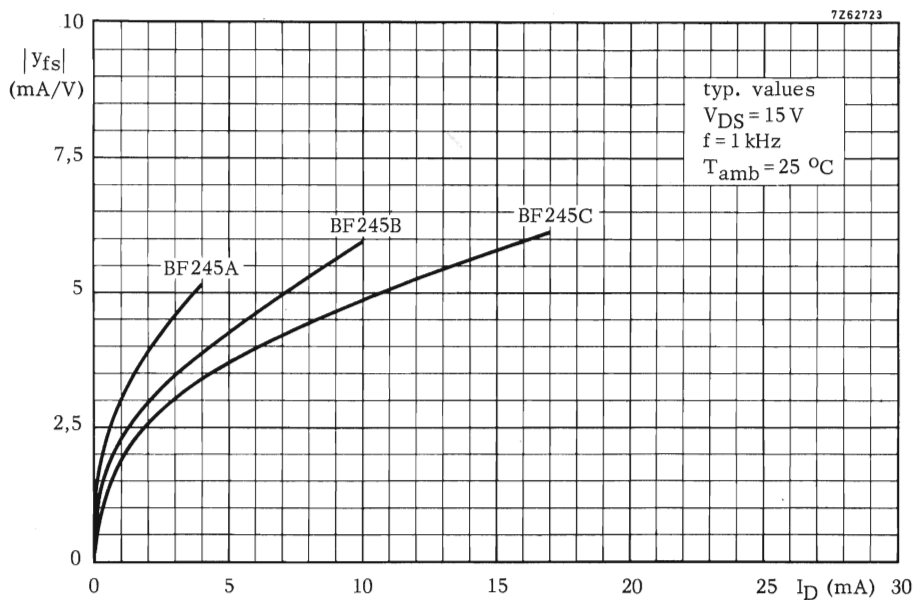


Fig. 15

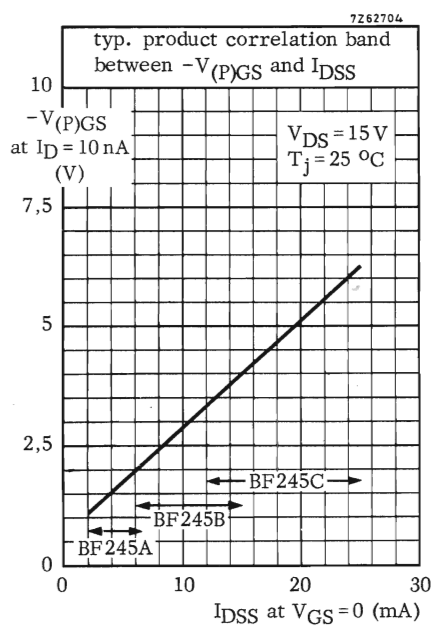


Fig. 16

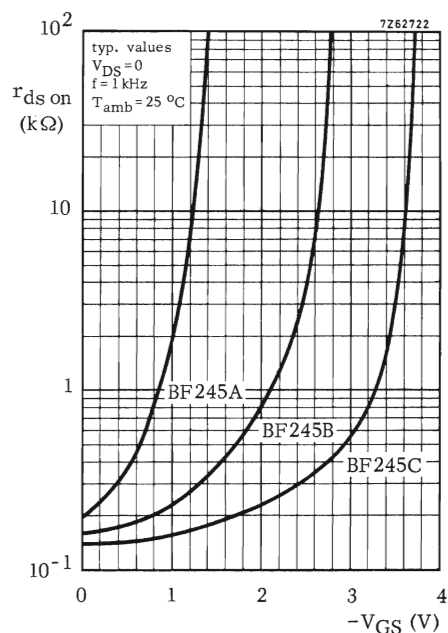


Fig. 17

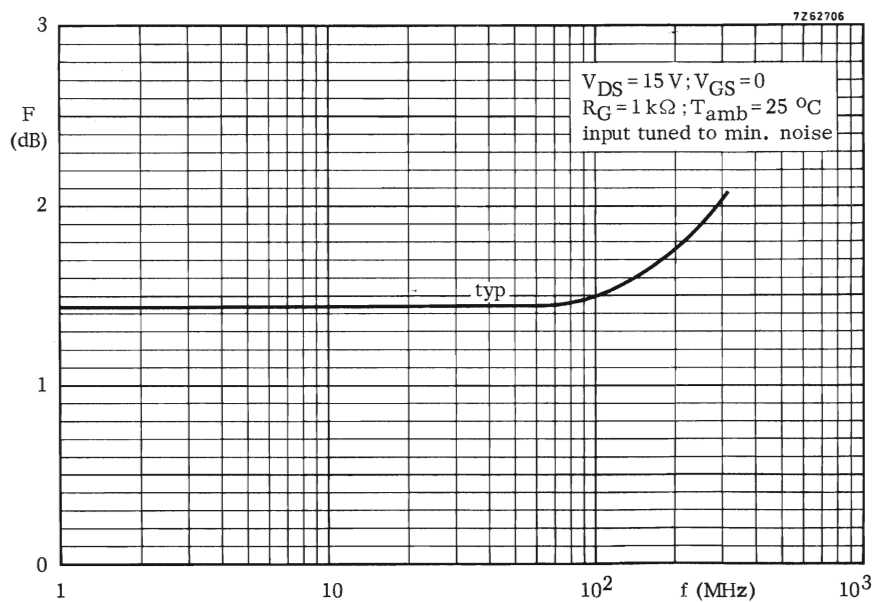


Fig. 18

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical n-channel planar epitaxial junction field-effect transistors in plastic TO-92 variants, intended for v.h.f. and u.h.f. amplifiers, mixers, and general purpose switching.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25 V		
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	250 mW		
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}		BF247A	B	C
		$>$	30	60	110 mA
		$<$	80	140	250 mA
Gate-source cut-off voltage $I_D = 10\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$		0,6 to 14,5 V		
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}$	C_{rs}	typ.	3,5 pF		
Transfer admittance (common source) $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	$>$	8 mS		

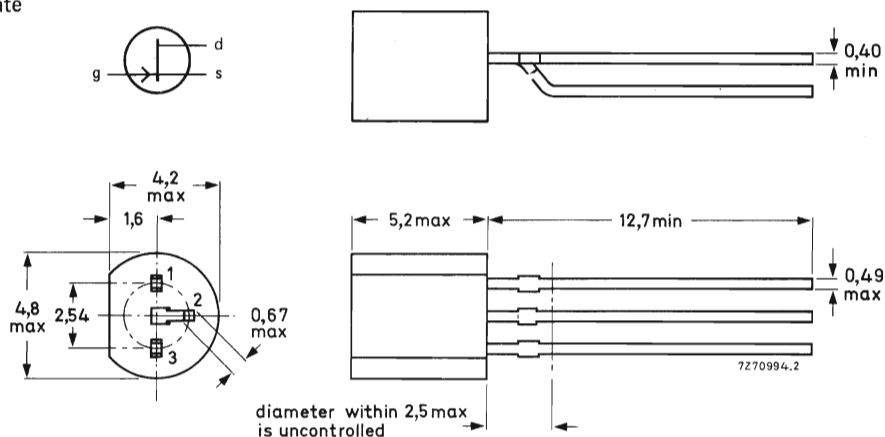
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

- 1 = drain
- 2 = source
- 3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate current	I_G	max.	10 mA
Total power dissipation up to $T_{amb} = 25^\circ\text{C}$	P_{tot}	max.	250 mW
Storage temperature	T_{stg}		-65 to $+150^\circ\text{C}$
Junction temperature	T_j	max.	150°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	500 K/W
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CHARACTERISTICS

 $T_{amb} = 25^\circ\text{C}$

	BF247A	B	C
Gate cut-off current $-V_{GS} = 15\text{ V}; V_{DS} = 0$	$-I_{GSS}$	< 5	5 nA
Drain current* $V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}	> 30 < 80	60 140 110 mA 250 mA
Gate-source breakdown voltage $-I_G = 1\ \mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	> 25	25 25 V
Gate-source voltage $I_D = 200\ \mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS}$	> 1,5 < 4,0	3,0 7,0 5,5 V 12,0 V
Gate-source cut-off voltage $I_D = 10\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$		0,6 to 14,5 V
Transfer admittance (common source) $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	> typ.	8 mS 17 mS
Capacitances at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}$			
feed-back capacitance	C_{rs}	typ.	3,5 pF
input capacitance	C_{is}	typ.	11 pF
output capacitance	C_{cs}	typ.	5 pF
Cut-off frequency** $V_{DS} = 15\text{ V}; V_{GS} = 0$	f_{gfs}	typ.	450 MHz

* Measured under pulse conditions; $t_p = 300\ \mu\text{s}$; $\delta \leq 0,02$.** The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for v.h.f. and u.h.f. applications.

QUICK REFERENCE DATA

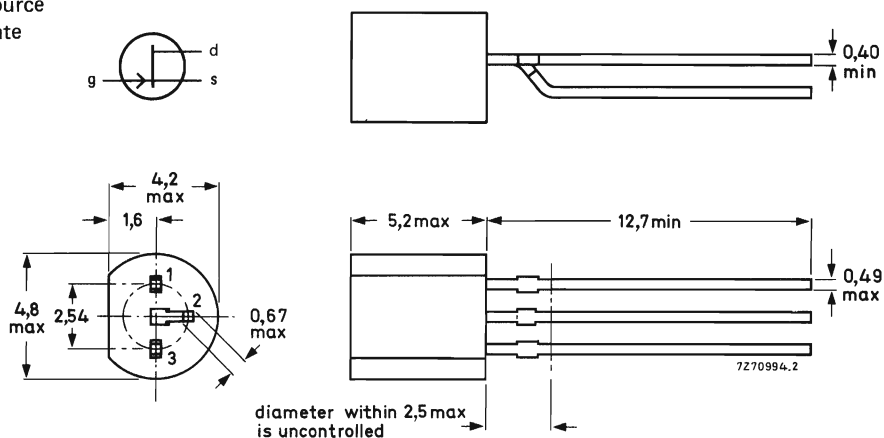
Drain-source voltage	$\pm V_{DS}$	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
Drain current			
$V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}	BF256A	
		> 3	6
		< 7	13
Feedback capacitance at $f = 1\text{ MHz}$			
$V_{DS} = 20\text{ V}; -V_{GS} = 1\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	C_{rs}	typ.	0,7 pF
Transfer admittance (common source)			
$V_{DS} = 15\text{ V}; V_{GS} = 0; f = 1\text{ kHz}; T_{amb} = 25\text{ }^{\circ}\text{C}$	$ Y_{fs} $	>	4,5 mS
Power gain at $f = 800\text{ MHz}$			
$V_{DS} = 15\text{ V}; R_S = 47\text{ }\Omega$	G_p	typ.	11 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning;
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Gate current	I_G	max.	10 mA
Total power dissipation			
up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
up to $T_{amb} = 90\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW 1)
Storage temperature	T_{stg}		-65 to $+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	$150\text{ }^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	250 K/W
From junction to ambient	$R_{th\ j-a}$	=	200 K/W 1)

CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off current

 $-V_{GS} = 20\text{ V}; V_{DS} = 0$ $-I_{GSS} < 5\text{ nA}$

Drain current 2)

 $V_{DS} = 15\text{ V}; V_{GS} = 0$

	BF256A	B	C
$I_{DSS\ 3)}$	> 3	6	11 mA
	< 7	13	18 mA

Gate-source breakdown voltage

 $-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$ $-V_{(BR)GSS} > 30\text{ V}$

Gate-source voltage

 $I_D = 200\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$ $-V_{GS\ 3)} 0,5\text{ to }7,5\text{ V}$

1) Transistor mounted on printed circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: $t_p = 300\text{ }\mu\text{s}; \delta \leq 0,02$.

3) BF256B/1: $I_{DSS} = 6\text{ to }8\text{ mA}; -V_{GS} = 1,4\text{ to }2,6\text{ V}$.

y-parameters (common source)

Transistor admittance at $f = 1 \text{ kHz}$ $V_{DS} = 15 \text{ V}; V_{GS} = 0$

$ y_{fs} $	>	4,5 mS	1)
	typ.	5 mS	1)

Output capacitance at $f = 1 \text{ MHz}$ $V_{DS} = 20 \text{ V}; V_{GS} = 0$

C_{os}	typ.	1,2 pF
----------	------	--------

Feedback capacitance at $f = 1 \text{ MHz}$ $V_{DS} = 20 \text{ V}; -V_{GS} = 1 \text{ V}$

C_{rs}	typ.	0,7 pF
----------	------	--------

Cut-off frequency

 $V_{DS} = 15 \text{ V}; V_{GS} = 0$

f_{gfs}	typ.	1 GHz	2)
-----------	------	-------	----

Noise figure at $f = 800 \text{ MHz}$ $V_{DS} = 10 \text{ V}; R_S = 47 \Omega$

F	typ.	7,5 dB
-----	------	--------

Power gain at $f = 800 \text{ MHz}$ $V_{DS} = 15 \text{ V}; R_S = 47 \Omega$

G_p	typ.	11 dB
-------	------	-------

1) Measured under pulse conditions: $t_p = 300 \mu\text{s}; \delta \leq 0,02$.2) The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

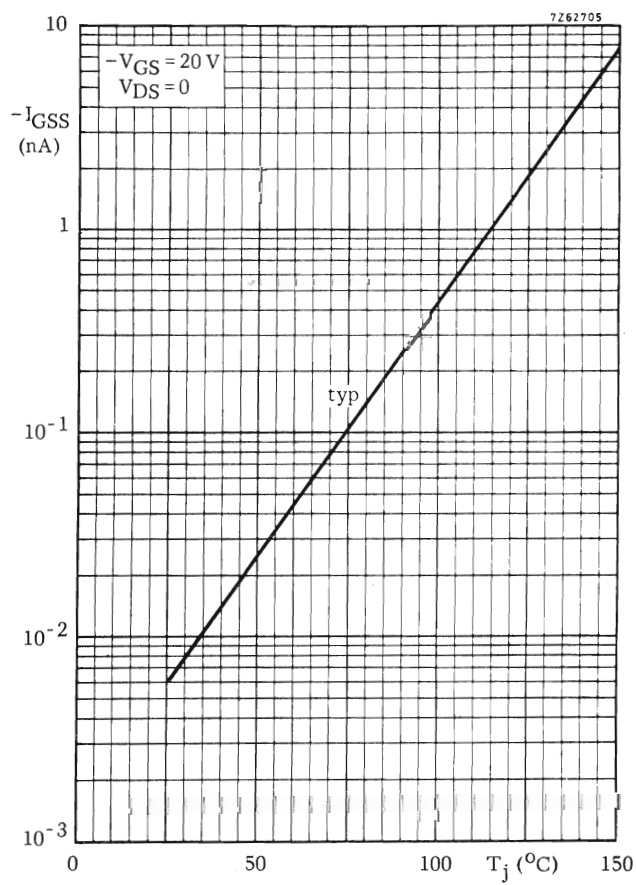


Fig. 2

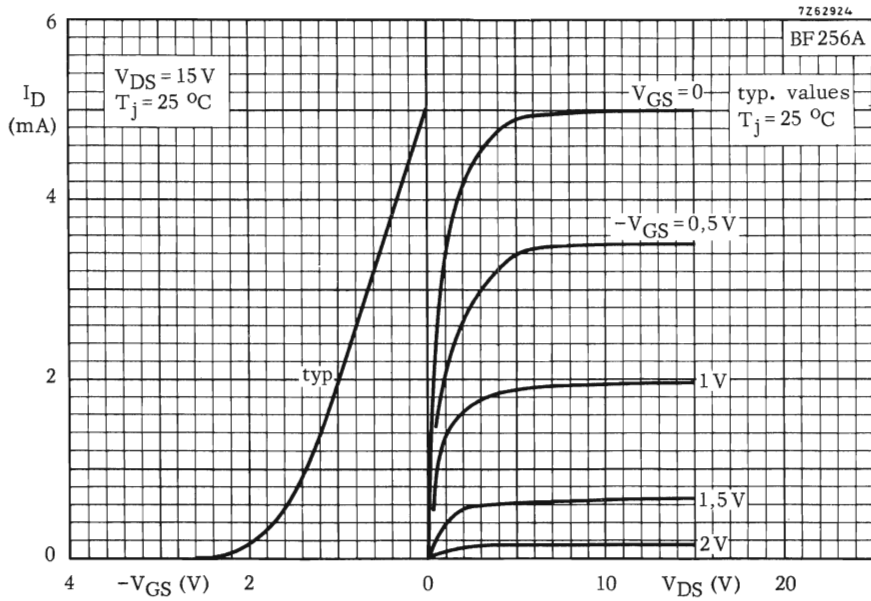


Fig. 3

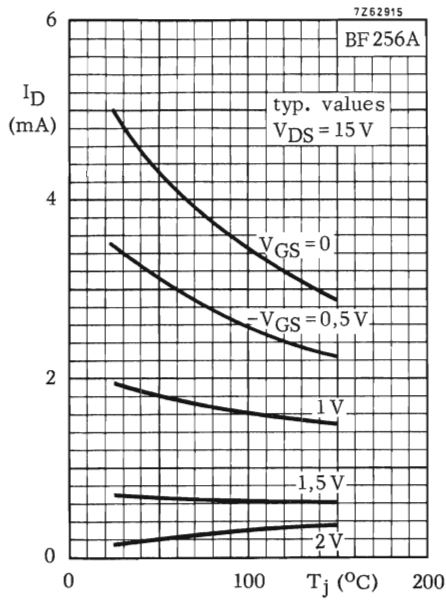


Fig. 4

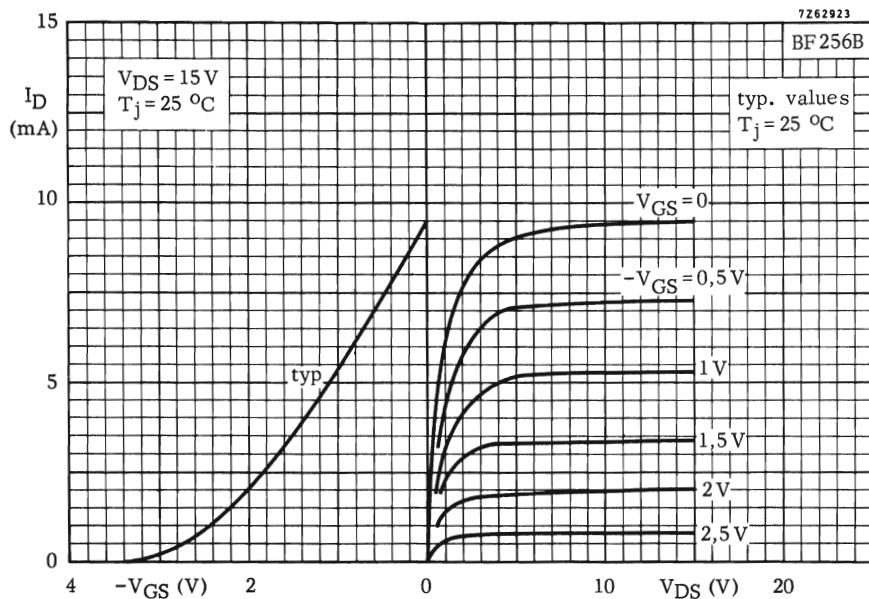


Fig. 5

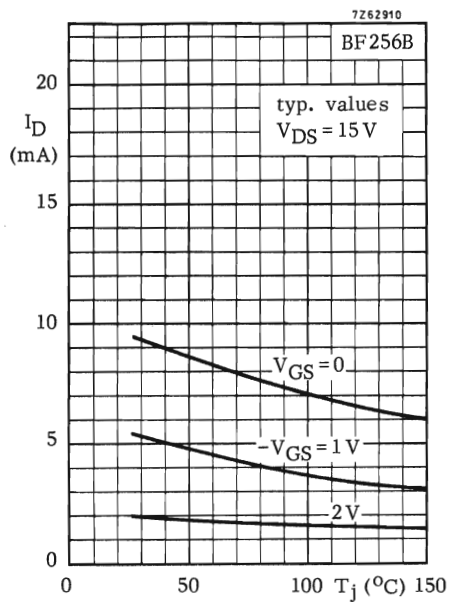


Fig. 6

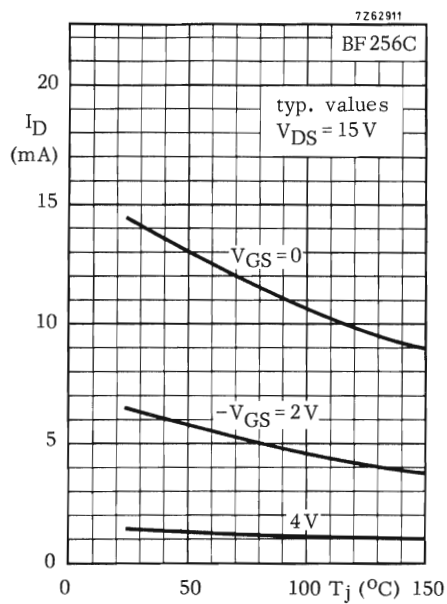
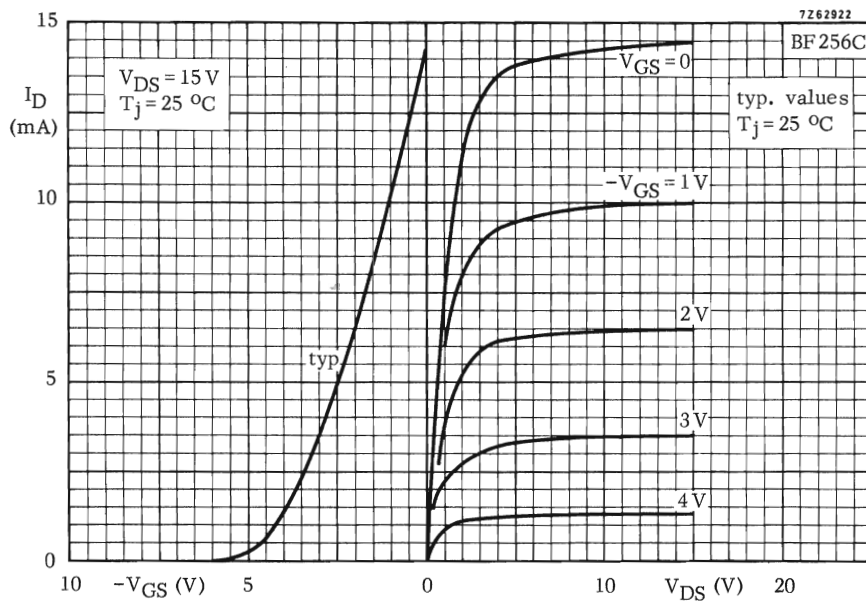


Fig. 8

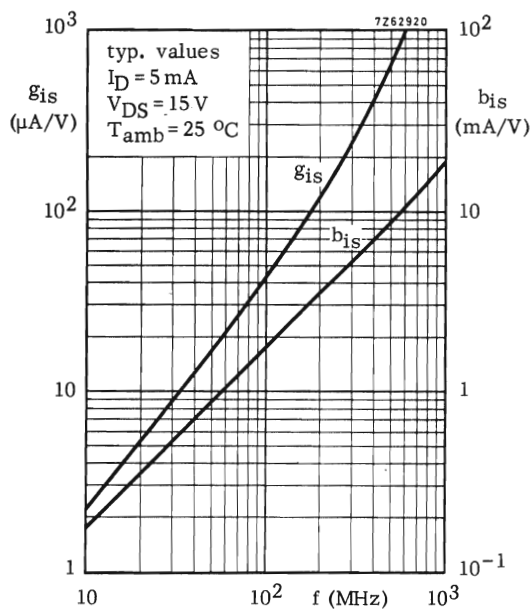


Fig. 9

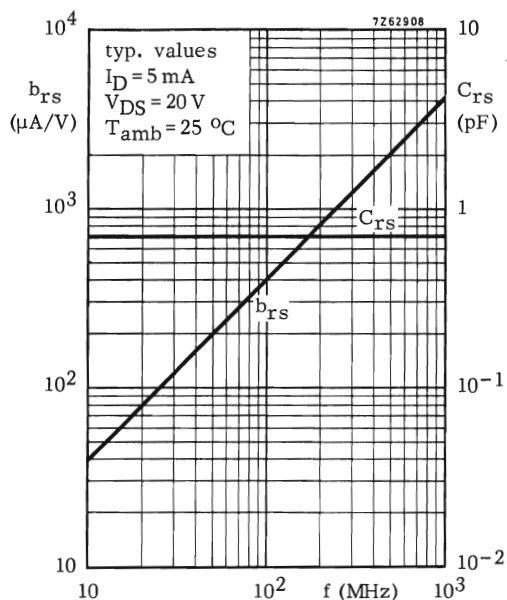


Fig. 10

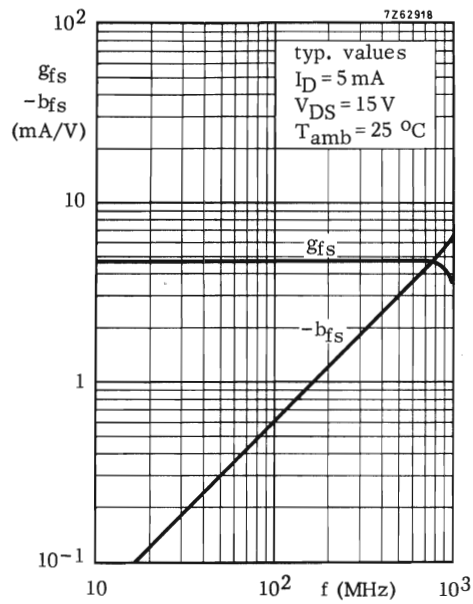


Fig. 11

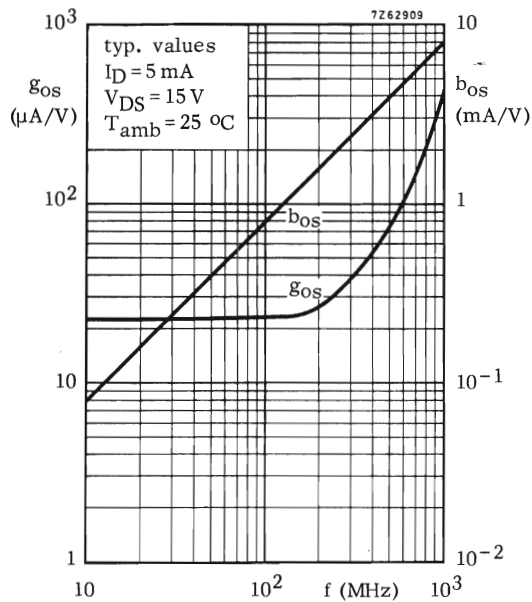


Fig. 12

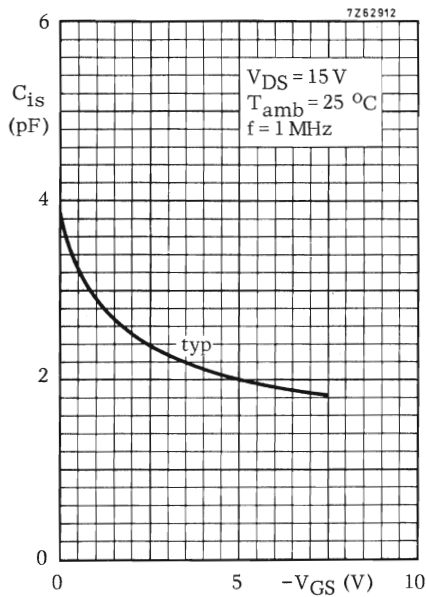


Fig. 13

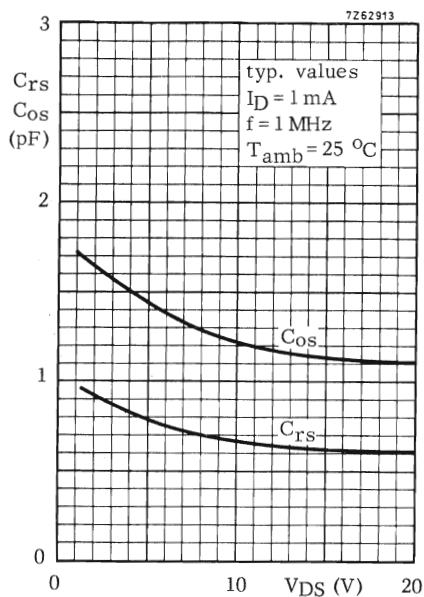


Fig. 14

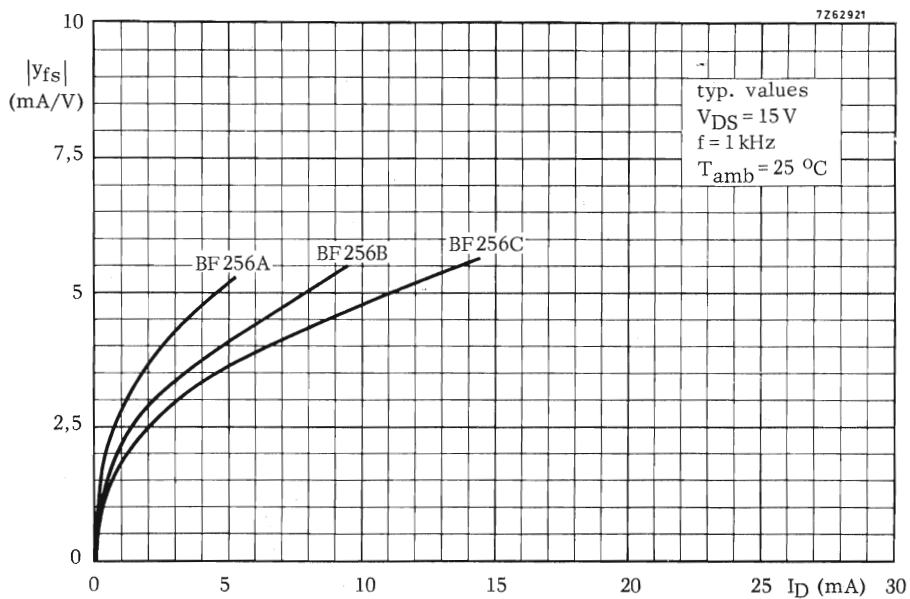


Fig. 15

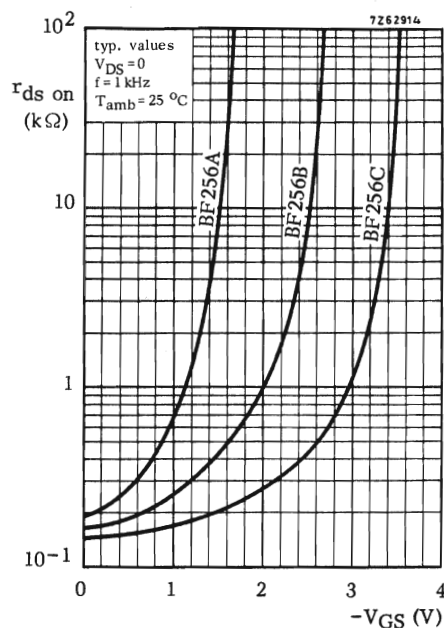


Fig. 16

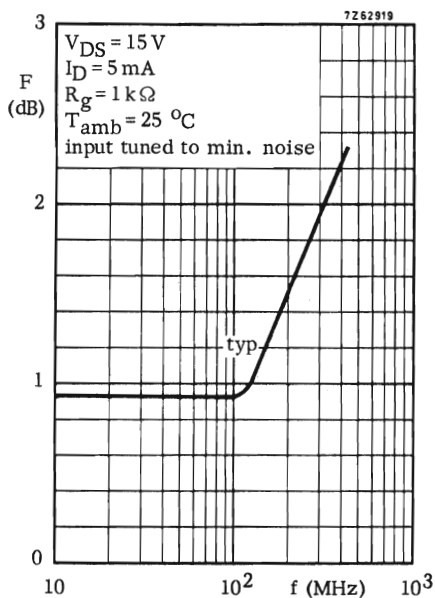


Fig. 17

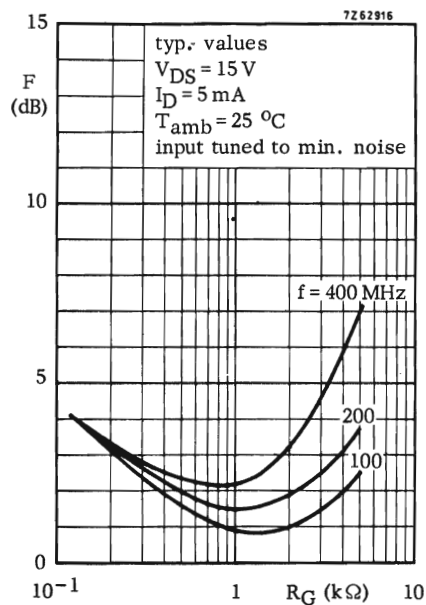


Fig. 18

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications up to the v.h.f. range.

These FETs can be supplied in four I_{DSS} groups. Special features are the low feedback capacitance and the low noise figure. Thanks to these special features the BF410 is very suitable for applications such as the r.f. stages in f.m. portables (type A), car radios (type B) and mains radios (type C) or the mixer stage (type D).

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V				
Drain current (d.c. or average)	I_D	max.	30	mA				
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	300	mW				
			BF410A	B	C	D		
Drain current $V_{DS} = 10\text{ V}; V_{GS} = 0$	I_{DSS}	>	0,7	2,5	6	10	mA	
		<	3,0	7,0	12	18	mA	
Transfer admittance (common source) $V_{DS} = 10\text{ V}; V_{GS} = 0; f = 1\text{ kHz}$		$ y_{fs} $	>	2,5	4	6	7	mS
Feedback capacitance $V_{DS} = 10\text{ V}; V_{GS} = 0$		C_{rs}	typ.	0,3	0,3	—	—	pF
$V_{DS} = 10\text{ V}; I_D = 5\text{ mA}$		C_{rs}	typ.	—	—	0,3	0,3	pF
Noise figure at optimum source admittance $G_S = 1\text{ mS}; -B_S = 3\text{ mS}; f = 100\text{ MHz}$		F	typ.	1,5	1,5	—	—	dB
$V_{DS} = 10\text{ V}; V_{GS} = 0$		F	typ.	—	—	1,5	1,5	dB
$V_{DS} = 10\text{ V}; I_D = 5\text{ mA}$		F	typ.	—	—	1,5	1,5	dB

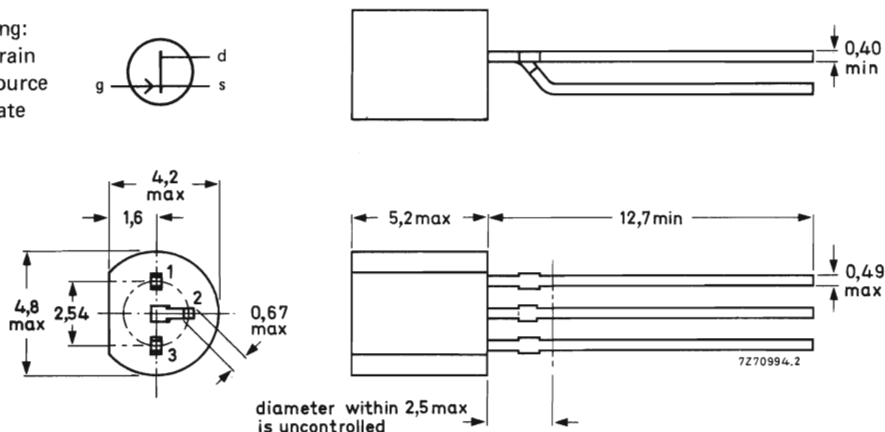
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

- 1 = drain
- 2 = source
- 3 = gate



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain-gate voltage (open source)	V_{DGO}	max.	20 V
Drain current (d.c. or average)	I_D	max.	30 mA
Gate current	$\pm I_G$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
Storage temperature	T_{stg}		-65 to $+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	$150\text{ }^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	250 K/W
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STATIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$

			BF410A	B	C	D
Gate cut-off current $-V_{GS} = 0,2\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	10	10	10	10 nA
Gate-drain breakdown voltage $I_S = 0; -I_D = 10\text{ }\mu\text{A}$	$-V_{(BR)GDO}$	>	20	20	20	20 V
Drain current $V_{DS} = 10\text{ V}; V_{GS} = 0$	I_{DSS}	> <	0,7 3,0	2,5 7,0	6 12	10 18 mA
Gate-source cut-off voltage $I_D = 10\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$	$-V_{(P)GS}$	typ.	0,8	1,5	2,2	3 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $V_{DS} = 10\text{ V}$; $V_{GS} = 0$; $T_{amb} = 25\text{ }^{\circ}\text{C}$ for **BF410A** and **B**

$V_{DS} = 10\text{ V}$; $I_D = 5\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$ for **BF410C** and **D**

y-parameters (common source)

			BF410A	B	C	D
Input capacitance at $f = 1\text{ MHz}$	C_{is}	<	5	5	5	5 pF
Input conductance at $f = 100\text{ MHz}$	g_{is}	typ.	100	90	60	50 μS
Feedback capacitance at $f = 1\text{ MHz}$	C_{rs}	typ.	0,3	0,3	0,3	0,3 pF
		<	0,4	0,4	0,4	0,4 pF
Transfer admittance at $f = 1\text{ kHz}$ $V_{GS} = 0$ instead of $I_D = 5\text{ mA}$	$ Y_{fs} $	>	2,5	4,0	4,0	3,5 mS
		>	—	—	6,0	7,0 mS
Transfer admittance at $f = 100\text{ MHz}$	$ Y_{fs} $	typ.	3,5	5,5	5,0	5,0 mS
Output capacitance at $f = 1\text{ MHz}$	C_{os}	<	3	3	3	3 pF
Output conductance at $f = 1\text{ MHz}$	g_{os}	<	60	80	100	120 μS
Output conductance at $f = 100\text{ MHz}$	g_{os}	typ.	35	55	70	90 μS
Noise figure at optimum source admittance $G_S = 1\text{ mS}$; $-B_S = 3\text{ mS}$; $f = 100\text{ MHz}$						
	F	typ.	1,5	1,5	1,5	1,5 dB

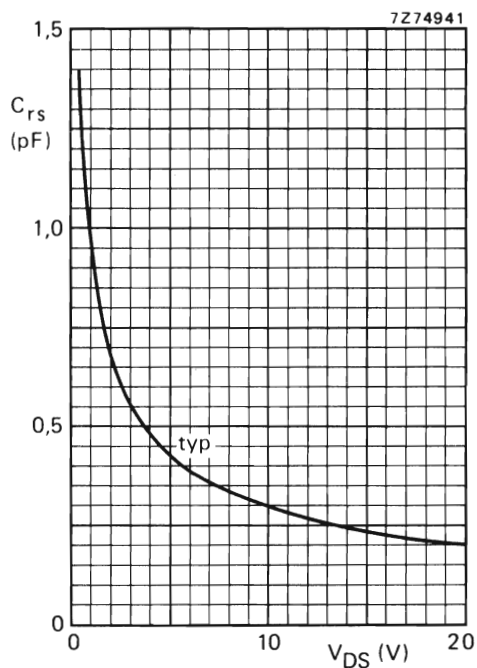


Fig. 2 $V_{GS} = 0$ for BF410A and BF410B;
 $I_D = 5$ mA for BF410C and BF410D;
 $f = 1$ MHz; $T_{amb} = 25$ °C.

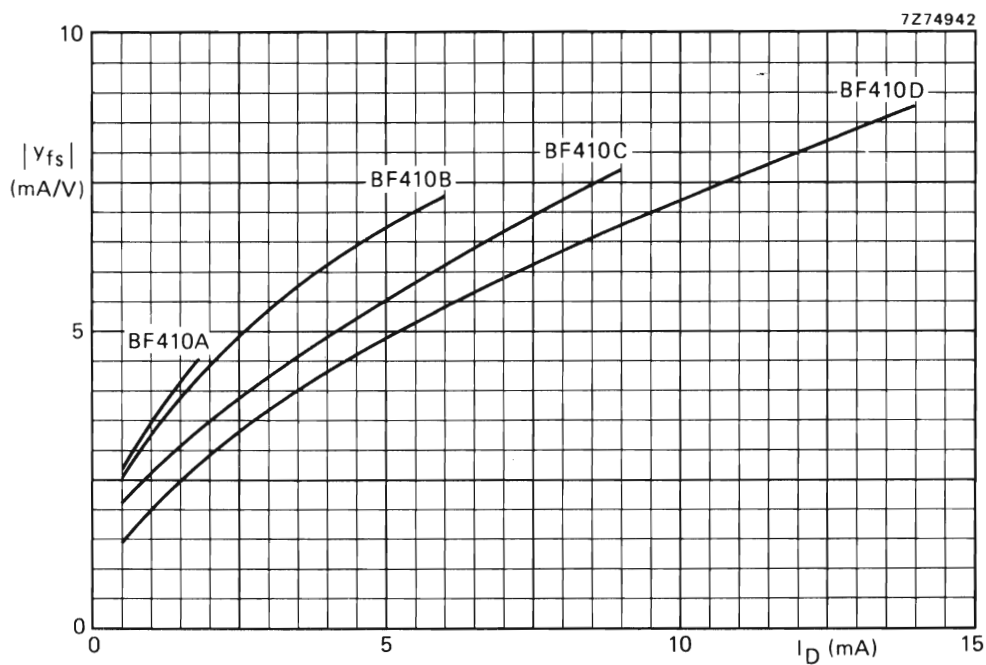


Fig. 3 $V_{DS} = 10$ V; $f = 1$ kHz; $T_{amb} = 25$ °C; typical values.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in the miniature plastic envelope intended for applications up to the v.h.f. range in hybrid thick and thin-film circuits. Special features are the low feedback capacitance and the low noise figure. These features make the product very suitable for applications such as the r.f. stages in f.m. portables (BF510), car radios (BF511) and mains radios (BF512) or the mixer stage (BF513).

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V		
Drain current (d.c. or average)	I_D	max.	30	mA		
Total power dissipation up to $T_{amb} = 65\text{ }^{\circ}\text{C}$	P_{tot}	max.	250	mW		
			BF510	511	512	513
Drain current $V_{DS} = 10\text{ V}; V_{GS} = 0$	I_{DSS}	$>$	0,7	2,5	6	10 mA
		$<$	3,0	7,0	12	18 mA
Transfer admittance (common source) $V_{DS} = 10\text{ V}; V_{GS} = 0; f = 1\text{ kHz}$	$ y_{fs} $	$>$	2,5	4	6	7 mS
Feedback capacitance $V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{rs}	typ.	0,3	0,3	—	— pF
$V_{DS} = 10\text{ V}; I_D = 5\text{ mA}$	C_{rs}	typ.	—	—	0,3	0,3 pF
Noise figure at optimum source admittance $G_S = 1\text{ mS}; -B_S = 3\text{ mS}; f = 100\text{ MHz}$						
$V_{DS} = 10\text{ V}; V_{GS} = 0$	F	typ.	1,5	1,5	—	— dB
$V_{DS} = 10\text{ V}; I_D = 5\text{ mA}$	F	typ.	—	—	1,5	1,5 dB

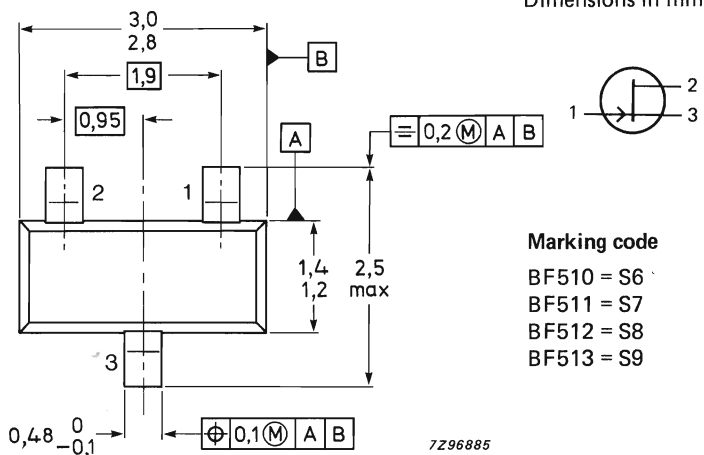
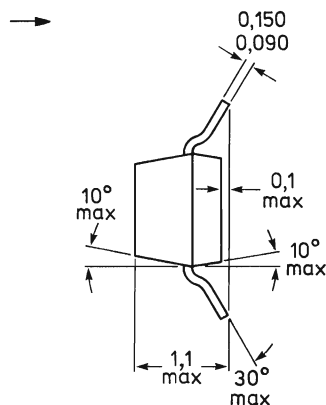
MECHANICAL DATA

SOT-23.

See also *Soldering recommendations*.

MECHANICAL DATA

Fig. 1 SOT-23



TOP VIEW

Marking code

BF510 = S6

BF511 = S7

BF512 = S8

BF513 = S9

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage see Fig. 4

 V_{DS} max. 20 V

Drain-gate voltage (open source) see Fig. 4

 V_{DGO} max. 20 V

Drain current (d.c. or average)

 I_D max. 30 mA

Gate current

 $\pm I_G$ max. 10 mATotal power dissipation up to $T_{amb} = 60^\circ\text{C}^{**}$ P_{tot} max. 250 mW

Storage temperature range

 T_{stg} -65 to $+175^\circ\text{C}$

Junction temperature

 T_j max. 175°C

THERMAL CHARACTERISTICS*

$$T_j = P \times (R_{th\ j-t} + R_{th\ t-s} + R_{th\ s-a}) + T_{amb}$$

Thermal resistance

From junction to tab

 $R_{th\ j-t}$ = 60 K/W

From tab to soldering points

 $R_{th\ t-s}$ = 280 K/W

From soldering points to ambient**

 $R_{th\ s-a}$ = 90 K/W* See *Thermal characteristics*.

** Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

STATIC CHARACTERISTICS

 $T_{amb} = 25^{\circ}\text{C}$

			BF510	511	512	513
Gate cut-off current						
$-V_{GS} = 0,2\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	10	10	10	10 nA
Gate-drain breakdown voltage						
$I_S = 0; -I_D = 10\text{ }\mu\text{A}$	$-V_{(BR)GDO}$	>	20	20	20	20 V
Drain current						
$V_{DS} = 10\text{ V}; V_{GS} = 0$	I_{DSS}	>	0,7	2,5	6	10 mA
		<	3,0	7,0	12	18 mA
Gate-source cut-off voltage						
$I_D = 10\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$	$-V_{(P)GS}$	typ.	0,8	1,5	2,2	3 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $V_{DS} = 10\text{ V}; V_{GS} = 0; T_{amb} = 25^{\circ}\text{C}$ for BF510 and BF511 $V_{DS} = 10\text{ V}; I_D = 5\text{ mA}; T_{amb} = 25^{\circ}\text{C}$ for BF512 and BF513

y-parameters (common source)

			BF510	511	512	513
Input capacitance at $f = 1\text{ MHz}$	C_{is}	<	5	5	5	5 pF
Input conductance at $f = 100\text{ MHz}$	g_{is}	typ.	100	90	60	50 μS
Feedback capacitance at $f = 1\text{ MHz}$	C_{rs}	typ.	0,3	0,3	0,3	0,3 pF
		<	0,4	0,4	0,4	0,4 pF
Transfer admittance at $f = 1\text{ kHz}$	$ Y_{fs} $	>	2,5	4,0	4,0	3,5 mS
$V_{GS} = 0$ instead of $I_D = 5\text{ mA}$	$ Y_{fs} $	>	—	—	6,0	7,0 mS
Transfer admittance at $f = 100\text{ MHz}$	$ Y_{fs} $	typ.	3,5	5,5	5,0	5,0 mS
Output capacitance at $f = 1\text{ MHz}$	C_{os}	<	3	3	3	3 pF
Output conductance at $f = 1\text{ MHz}$	g_{os}	<	60	80	100	120 μS
Output conductance at $f = 100\text{ MHz}$	g_{os}	typ.	35	55	70	90 μS
Noise figure at optimum source admittance						
$G_S = 1\text{ mS}; -B_S = 3\text{ mS};$						
$f = 100\text{ MHz}$	F	typ.	1,5	1,5	1,5	1,5 dB

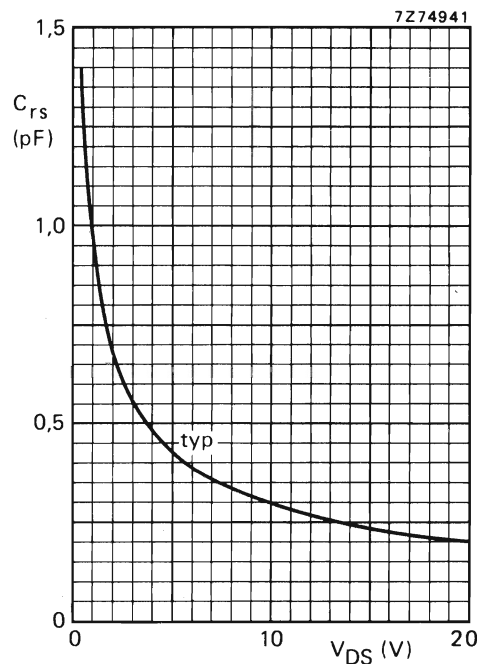


Fig. 2 $V_{GS} = 0$ for BF510 and BF511;
 $I_D = 5$ mA for BF512 and BF513;
 $f = 1$ MHz; $T_{amb} = 25$ °C.

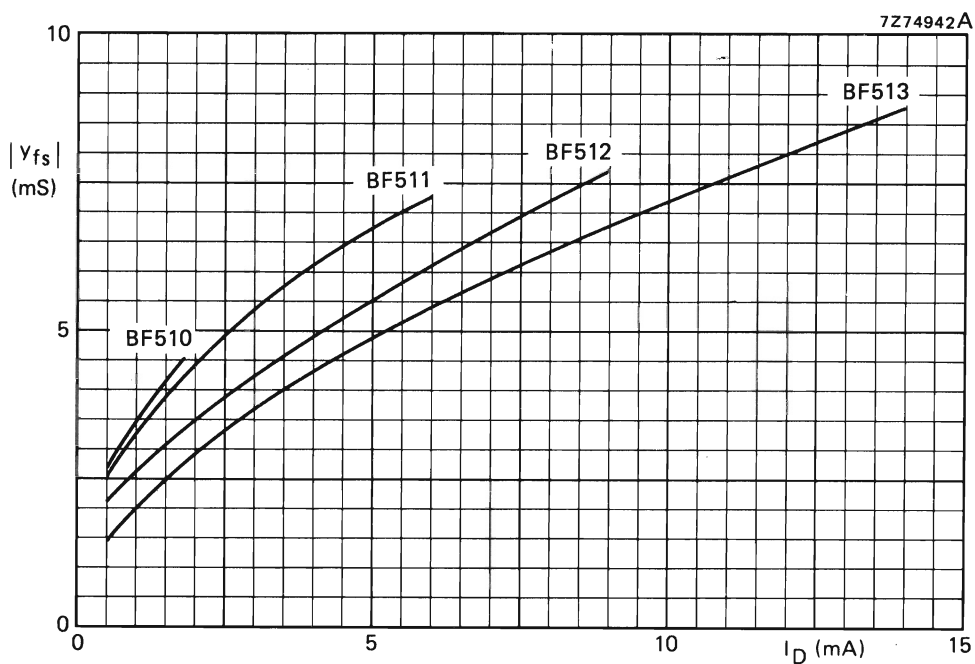


Fig. 3 $V_{DS} = 10$ V; $f = 1$ kHz; $T_{amb} = 25$ °C; typical values.

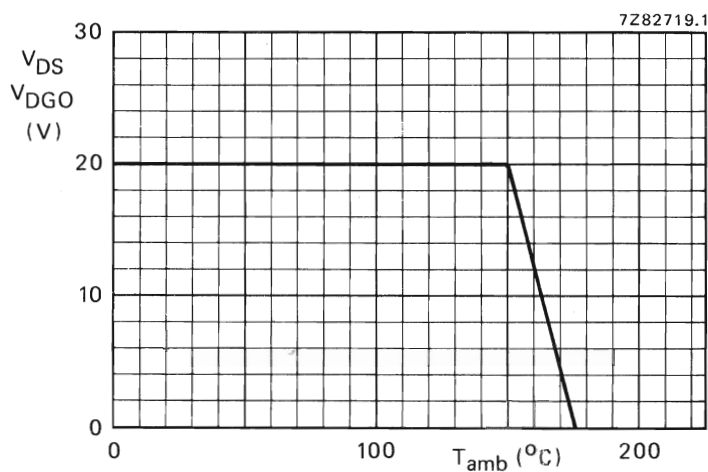


Fig. 4 Voltage derating curve.

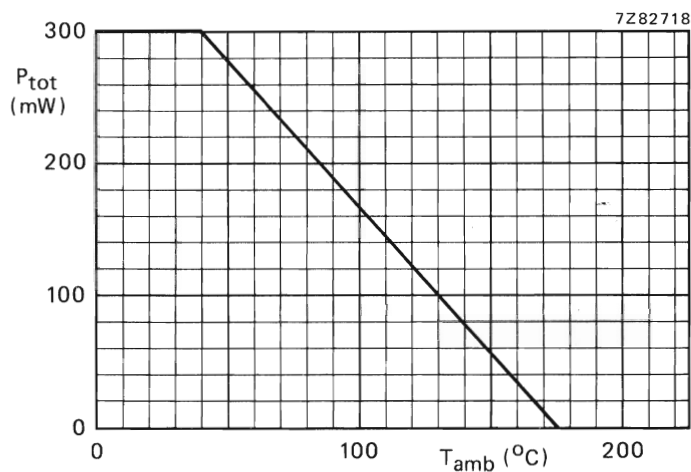


Fig. 5 Power derating curve.

DUAL N-CHANNEL FETS

Dual symmetrical n-channel silicon planar epitaxial junction field-effect transistors in a TO-71 metal envelope, with electrically insulated gates and a common substrate connected to the envelope; intended for high performance low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$; $I_D = 200\text{ }\mu\text{A}$; $V_{DG} = 15\text{ V}$

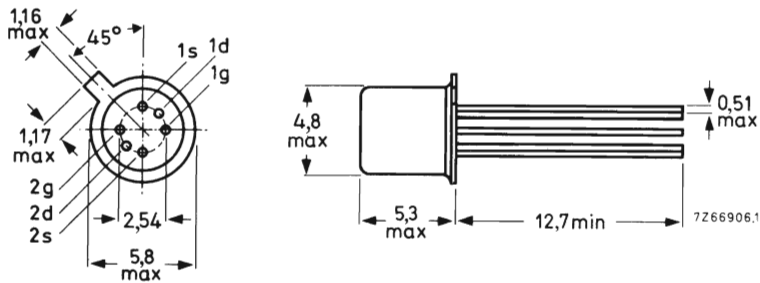
		BFQ10	11	12	13	14	15	16	
Difference in gate current	$ \Delta I_G $	< 10	10	10	10	10	10	10	pA
Gate-source voltage difference	$ \Delta V_{GS} $	< 5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left \frac{d\Delta V_{GS}}{dT} \right $	< 5	5	10	20	20	40	50	$\mu\text{V/K}$
Transfer conductance ratio	$\frac{g_{1f}}{g_{2f}}$	> 0,98	0,98	0,98	0,98	0,98	0,95	0,95	Ω
	$\frac{g_{2f}}{g_{1f}}$	< 1,02	1,02	1,02	1,02	1,02	1,05	1,05	
Difference in transfer impedance	$\left \Delta \frac{1}{g_{fs}} \right $	< 6	6	12	12	12	20	30	Ω
Difference in penetration factor	$\left \Delta \frac{g_{os}}{g_{fs}} \right $	< 10	30	40	50	60	70	100	$\mu\text{V/V}$
Common mode rejection ratio	CMRR	> 100	90	90	90	90	90	80	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-71.

All leads insulated from the case.



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Voltage between gate 1 and gate 2	$\pm V_{1G-2G}$	max.	40	V

Drain current	I_D	max.	30	mA
Gate current	I_G	max.	10	mA

Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	250	mW
--	-----------	------	-----	----

Storage temperature	T_{stg}	-65 to +200	$^{\circ}\text{C}$
---------------------	-----------	-------------	--------------------

Junction temperature	T_j	max.	200	$^{\circ}\text{C}$
----------------------	-------	------	-----	--------------------

THERMAL RESISTANCE

→ From junction to ambient in free air	$R_{th\ j-a}$	=	500	K/W
--	---------------	---	-----	-----

CHARACTERISTICS (total device)

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Measured at: $I_D = 200\text{ }\mu\text{A}$; $V_{DG} = 15\text{ V}$ except for drain current ratio.

Drain current ratio 1)		BFQ10	11	12	13	14	15	16	
$V_{DG} = 15\text{ V}$; $V_{GS} = 0$	$\frac{I_{1D-1SS}}{I_{2D-2SS}}$	$> 0,97$	0,95	0,95	0,95	0,92	0,90	0,80	
		$< 1,03$	1,05	1,05	1,05	1,08	1,10	1,20	
Difference in gate current	$ \Delta I_G $	< 10	10	10	10	10	10	10	pA
Gate-source voltage difference	$ \Delta V_{GS} $	< 5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left \frac{d \Delta V_{GS}}{dT} \right $	< 5	5	10	20	20	40	50	$\mu\text{V/K}$
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	$> 0,98$	0,98	0,98	0,98	0,98	0,95	0,95	
		$< 1,02$	1,02	1,02	1,02	1,02	1,05	1,05	
Difference in transfer impedance 2)	$\left \Delta \frac{1}{g_{fs}} \right $	< 6	6	12	12	12	20	30	Ω
Difference in penetration factor 3)	$\left \Delta \frac{g_{os}}{g_{fs}} \right $	< 10	30	40	50	60	70	100	$\mu\text{V/V}$
Common mode rejection ratio 4)	CMRR	> 100	90	90	90	90	90	80	dB

1) Measured under pulse conditions.

2) The difference in transfer impedance is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$$\left(\Delta \frac{1}{g_{fs}} = \frac{d \Delta V_{GS}}{d I_D} \text{ at } V_{DG} = \text{constant} \right)$$

3) The difference in penetration factor is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$$\left(\Delta \frac{g_{os}}{g_{fs}} = \frac{d \Delta V_{GS}}{d V_{DG}} \text{ at } I_D = \text{constant} \right)$$

4) Common mode rejection ratio

$$\text{CMRR (in dB)} = -20 \log \left| \Delta \frac{g_{os}}{g_{fs}} \right|$$

CHARACTERISTICS (Individual transistor) $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off current

$-V_{GS} = 20\text{ V}; V_{DS} = 0$

$-I_{GSS} < 100\text{ pA}$

$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_{amb} = 125\text{ }^{\circ}\text{C}$

$-I_{GSS} < 20\text{ nA}$

Gate current

$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}; T_{amb} = 125\text{ }^{\circ}\text{C}$

$I_G < 10\text{ nA}$

Drain current

$V_{DS} = 15\text{ V}; V_{GS} = 0$

$I_{DSS} 0,5\text{ to }10\text{ mA }^1)$

Gate-source voltage

$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$

$-V_{GS} < 2,7\text{ V}$

Gate-source cut-off voltage

$I_D = 1\text{ nA}; V_{DG} = 15\text{ V}$

$-V_{(P)GS} 0,5\text{ to }3,5\text{ V}$

Transfer conductance at $f = 1\text{ kHz}$

$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$

$g_{fs} > 1,0\text{ mS}$

Output conductance at $f = 1\text{ kHz}$

$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$

$g_{os} < 5\text{ }\mu\text{S}$

Input capacitance at $f = 1\text{ MHz}$

$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$

$C_{is} < 8\text{ pF }^2)$

Feedback capacitance at $f = 1\text{ MHz}$

$I_D = 200\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$

$C_{rs} < 1,0\text{ pF }^2)$

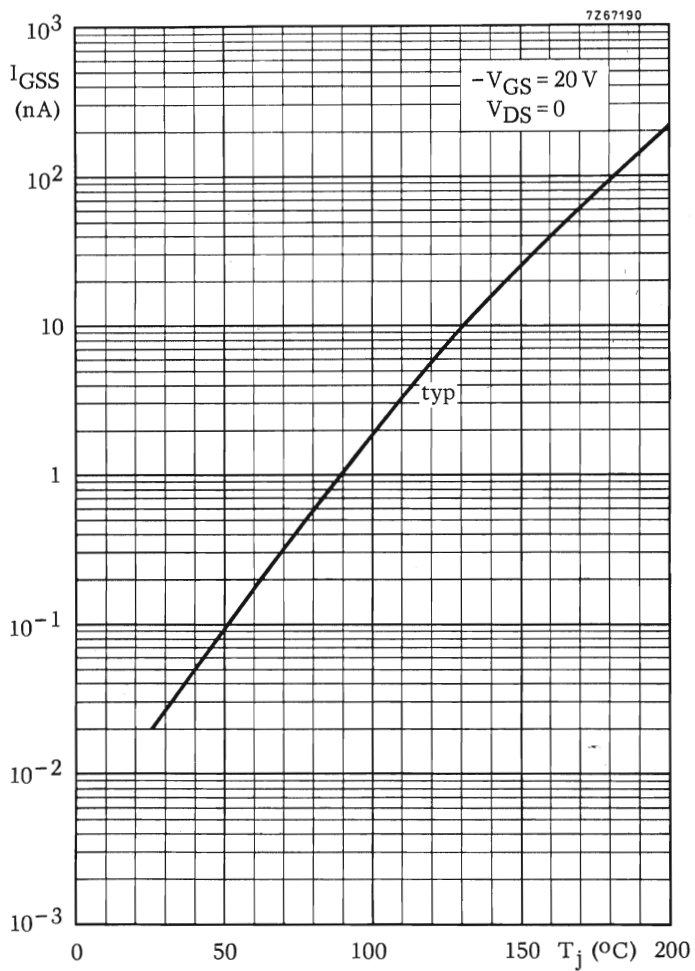
Equivalent noise voltage

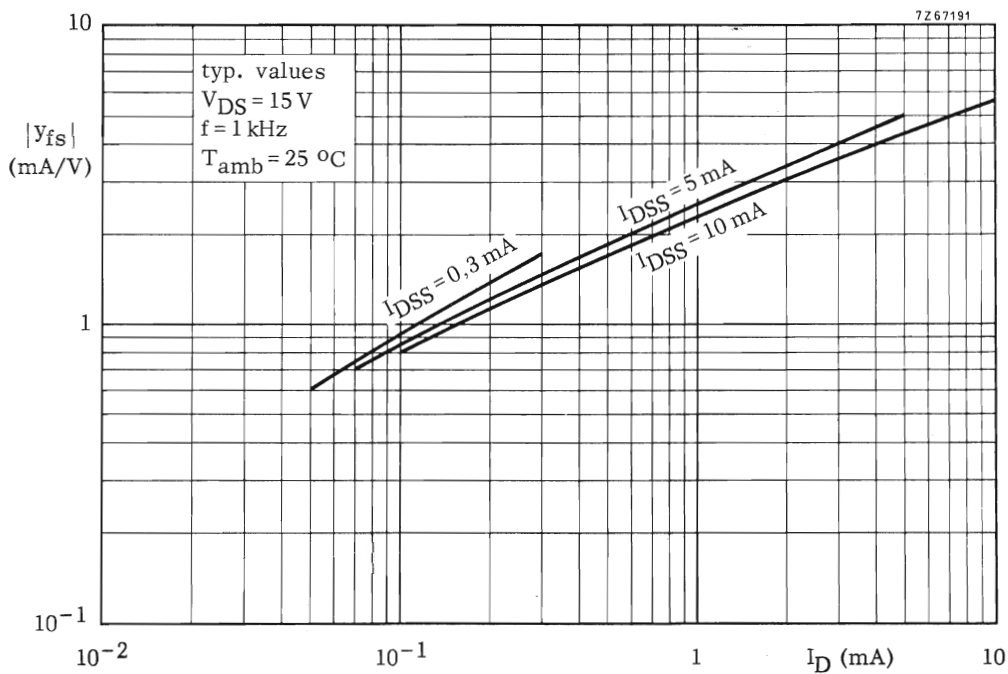
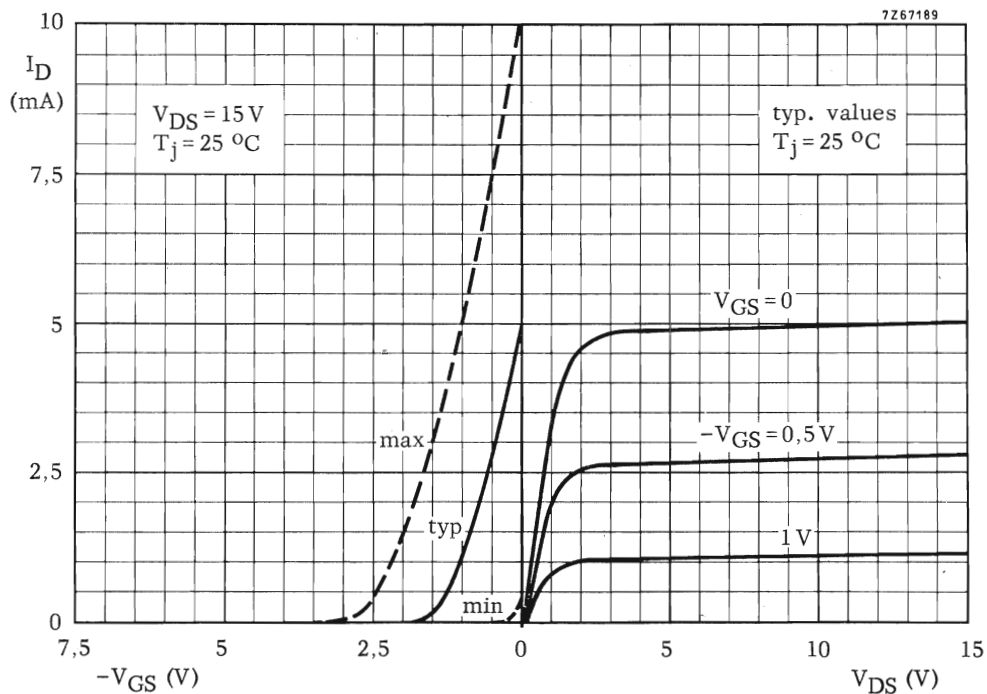
$I_D = 200\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$

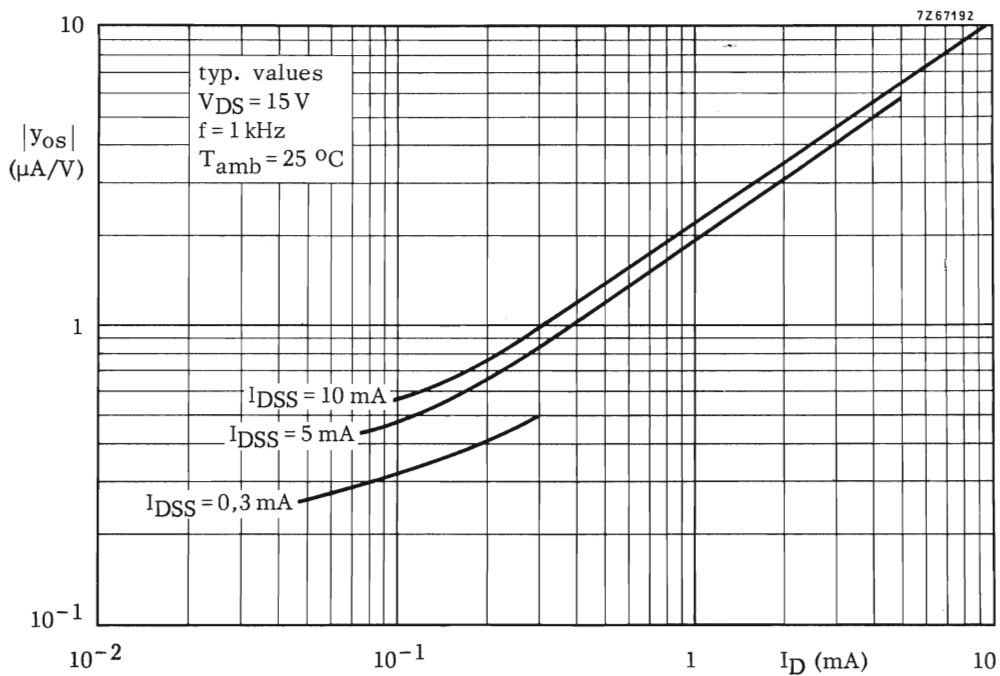
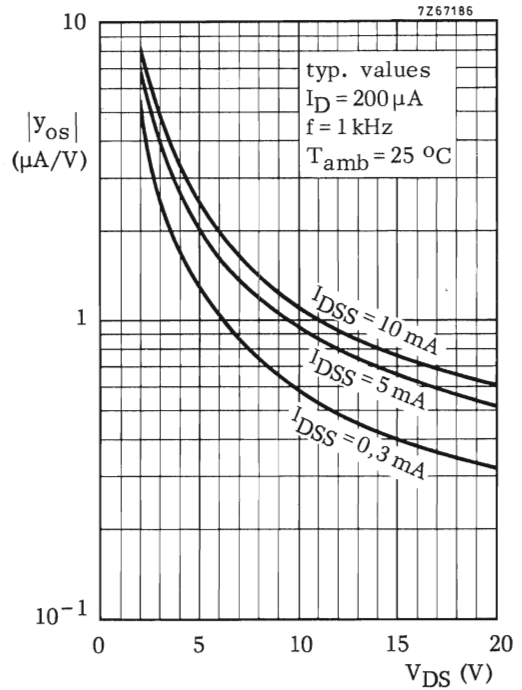
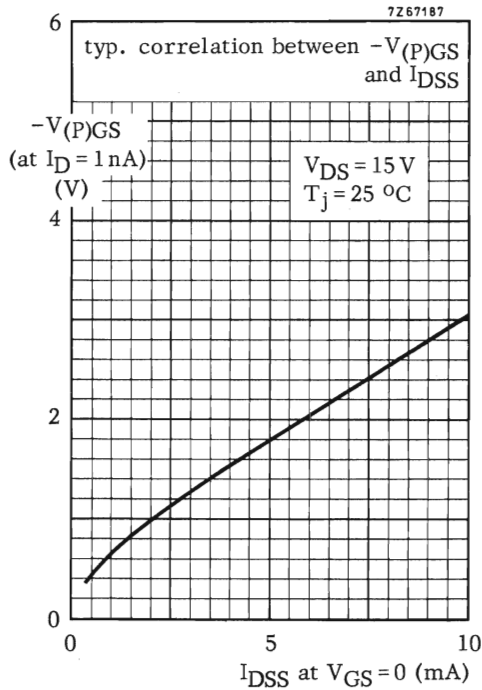
$B = 0,6\text{ to }100\text{ Hz}$

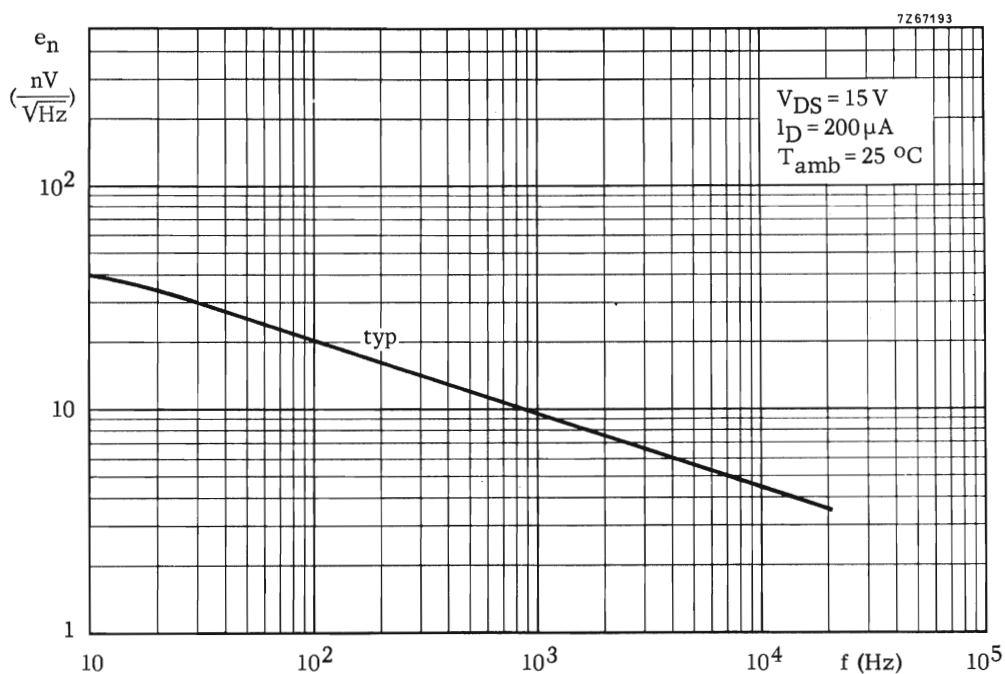
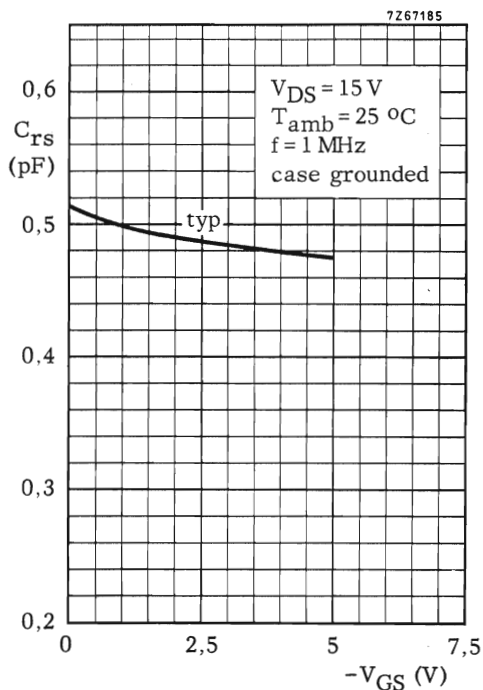
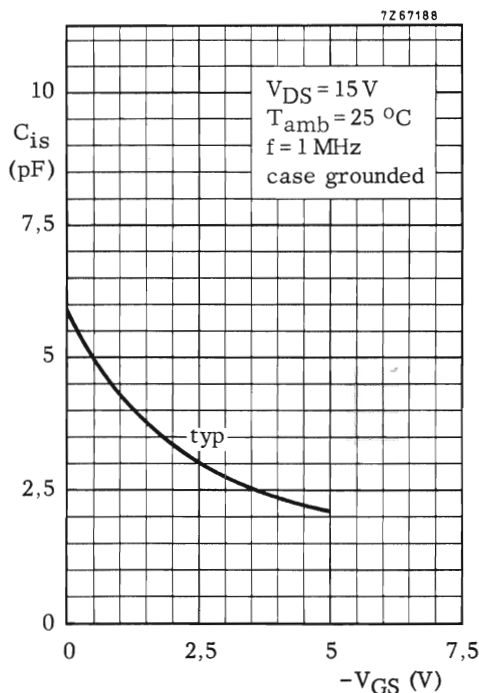
$V_n < 0,5\text{ }\mu\text{V}$

¹⁾ Measured under pulse conditions.²⁾ Measured with case grounded.









N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Planar epitaxial symmetrical junction field effect transistor in a microminiature plastic envelope. It is intended for low level general purpose amplifiers in thick and thin-film circuits.

QUICK REFERENCE DATA

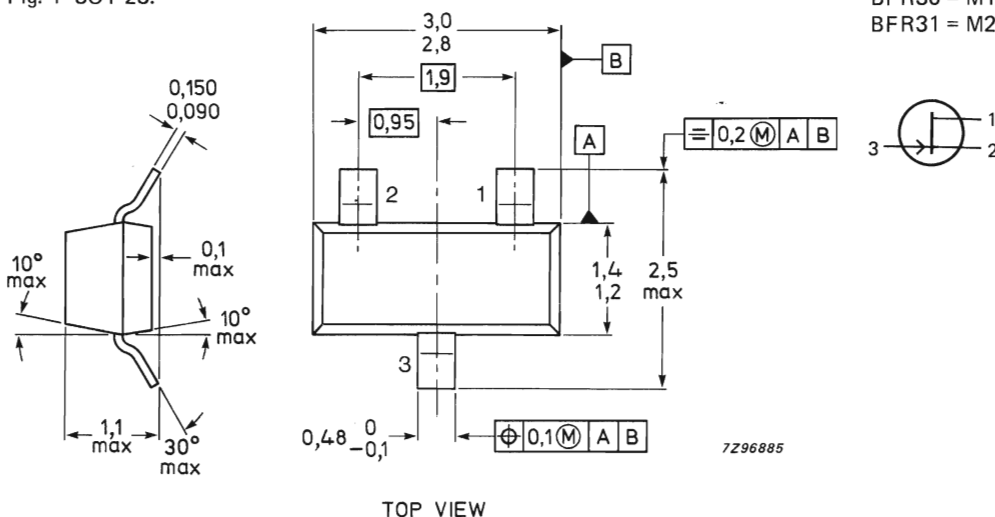
Drain-source voltage	$\pm V_{DS}$	max.	25	V	
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V	
Total power dissipation up to $T_{amb} = 65\text{ }^{\circ}\text{C}$	P_{tot}	max.	250	mW	
			BFR30	BFR31	
Drain current $V_{DS} = 10\text{ V}; V_{GS} = 0$	I_{DSS}	$>$	4	1	mA
		$<$	10	5	mA
Transfer admittance (common source) $I_D = 1\text{ mA}; V_{DS} = 10\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	$>$	1,0	1,5	mS
		$<$	4,0	4,5	mS

MECHANICAL DATA

Fig. 1 SOT-23.

Dimensions in mm

Marking code

BFR30 = M1
BFR31 = M2

Note: Drain and source are interchangeable.

See also *Soldering recommendations*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage see Fig. 2	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source) see Fig. 2	V_{DGO}	max.	25	V
Gate-source voltage (open drain) see Fig. 2	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to $T_{amb} = 65\text{ }^{\circ}\text{C}^{**}$	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		-65 to + 175	$^{\circ}\text{C}$
Junction temperature	T_j	max.	175	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS*

$$T_j = P \times (R_{th\ j-t} + R_{th\ t-s} + R_{th\ s-a}) + T_{amb}$$

Thermal resistance

From junction to tab	$R_{th\ j-t}$	=	60	K/W
From tab to soldering points	$R_{th\ t-s}$	=	280	K/W
From soldering points to ambient**	$R_{th\ s-a}$	=	90	K/W

CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

			BFR30	BFR31	
Gate cut-off current					
$-V_{GS} = 10\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	0,2	0,2	nA
Drain current					
$V_{DS} = 10\text{ V}; V_{GS} = 0$	I_{DSS}	>	4	1	mA
		<	10	5	mA
Gate-source voltage					
$I_D = 1\text{ mA}; V_{DS} = 10\text{ V}$	$-V_{GS}$	>	0,7	0	V
		<	3,0	1,3	V
$I_D = 50\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$	$-V_{GS}$	<	4,0	2,0	V
Gate-source cut-off voltage					
$I_D = 0,5\text{ nA}; V_{DS} = 10\text{ V}$	$-V_{(P)GS}$	<	5	2,5	V
y parameters					
Transfer admittance at $f = 1\text{ kHz}; T_{amb} = 25\text{ }^{\circ}\text{C}$					
$I_D = 1\text{ mA}; V_{DS} = 10\text{ V}$	$ Y_{fs} $	>	1,0	1,5	mS
		<	4,0	4,5	mS
$I_D = 200\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$	$ Y_{fs} $	>	0,5	0,75	mS
Output admittance at $f = 1\text{ kHz}$					
$I_D = 1\text{ mA}; V_{DS} = 10\text{ V}$	$ Y_{os} $	<	40	25	μS
$I_D = 200\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$	$ Y_{os} $	<	20	15	μS

* See *Thermal characteristics*.

** Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

y parameters (continued)

Input capacitance at $f = 1\text{ MHz}$

$I_D = 1\text{ mA}; V_{DS} = 10\text{ V}$

$I_D = 200\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$

Feedback capacitance at $f = 1\text{ MHz}; T_{\text{amb}} = 25\text{ }^\circ\text{C}$

$I_D = 1\text{ mA}; V_{DS} = 10\text{ V}$

$I_D = 200\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$

Equivalent noise voltage

$I_D = 200\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$

$B = 0,6\text{ to }100\text{ Hz}$

		BFR30	BFR31	
C_{is}	<	4	4	pF
C_{is}	<	4	4	pF
C_{rs}	<	1,5	1,5	pF
C_{rs}	<	1,5	1,5	pF
V_n	<	0,5	0,5	μV

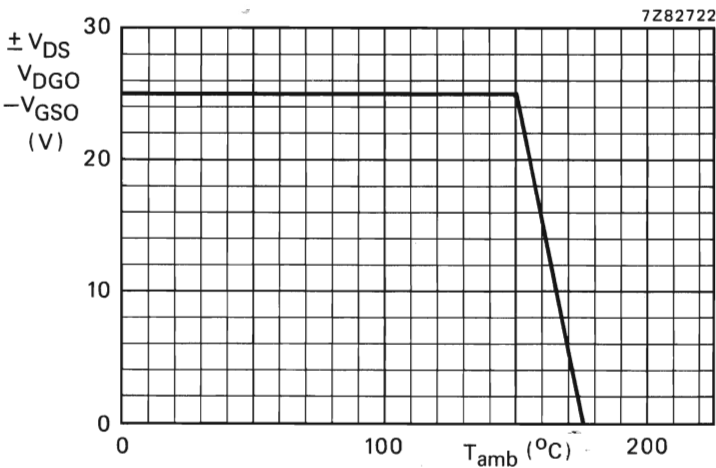


Fig. 2 Voltage derating curve.

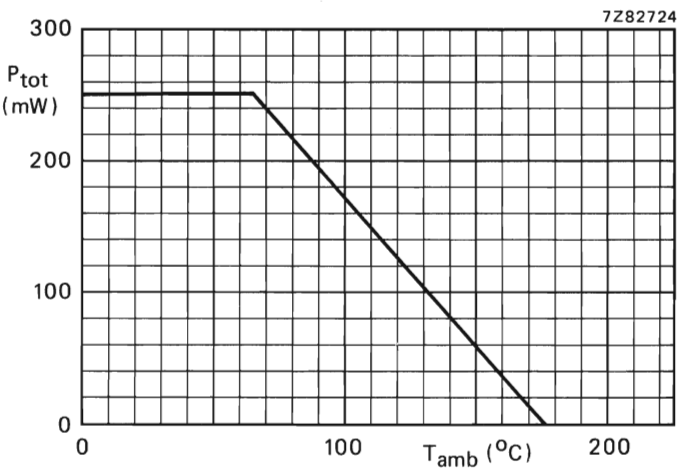


Fig. 3 Power derating curve.

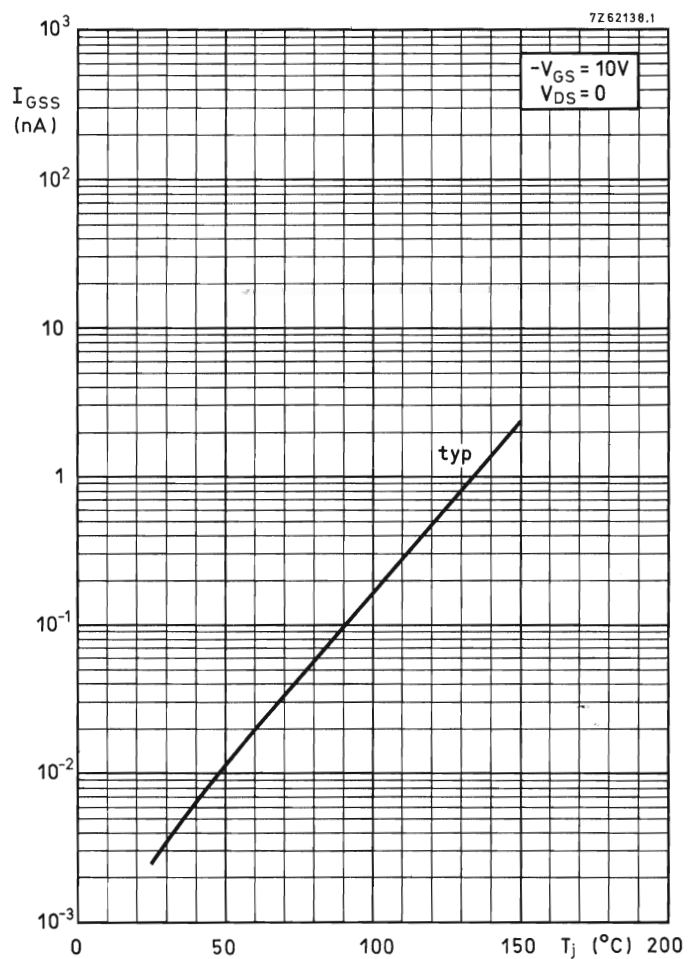


Fig. 4.

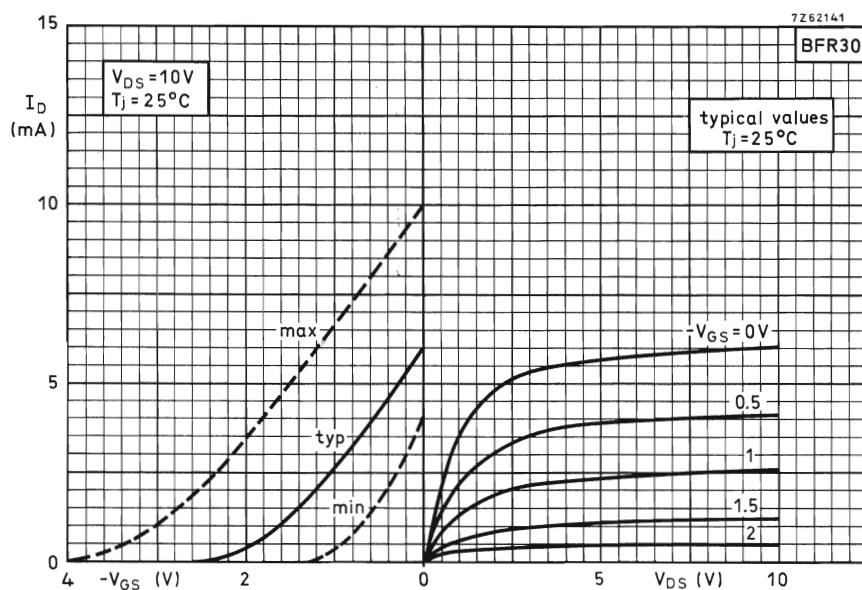


Fig. 5.

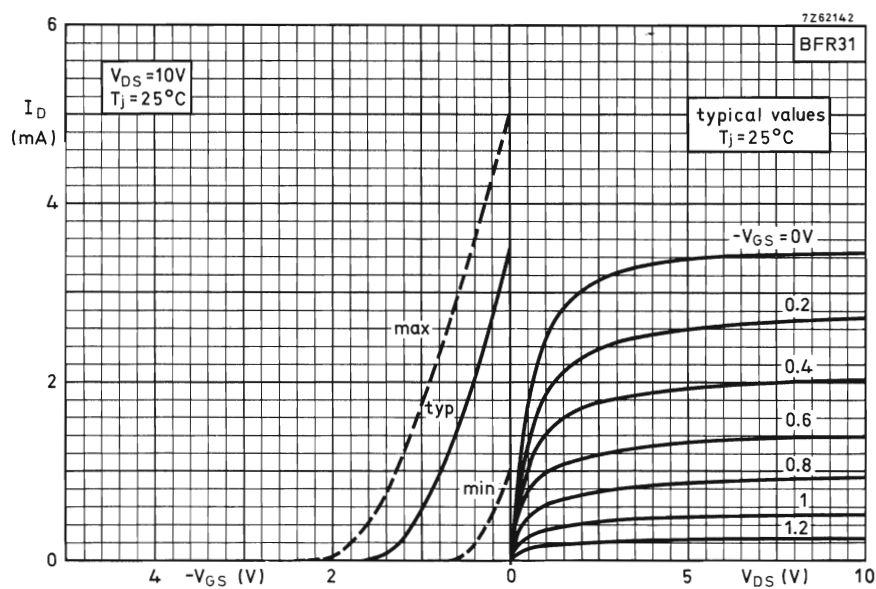


Fig. 6.

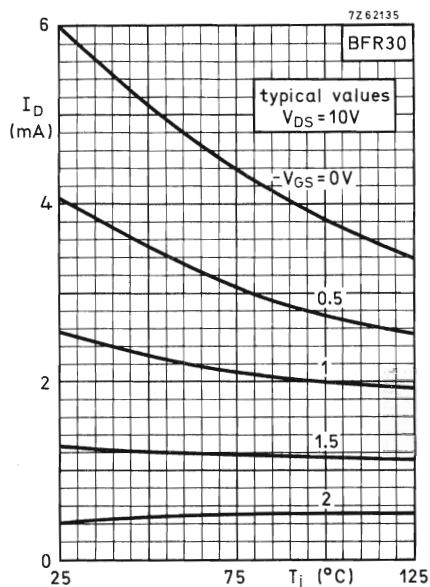


Fig. 7.

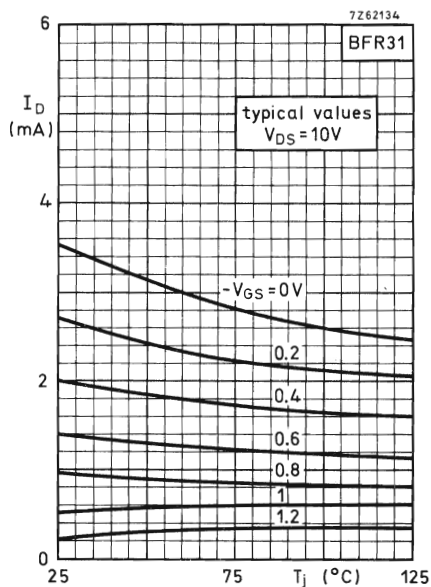


Fig. 8.

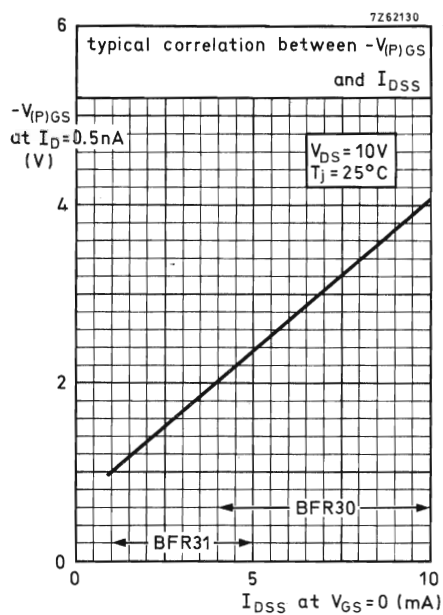


Fig. 9.

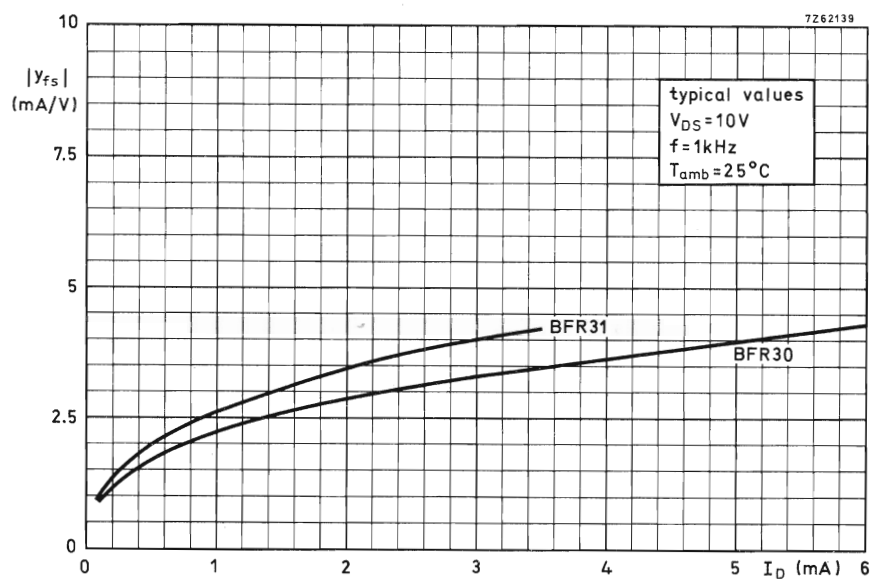


Fig. 10.

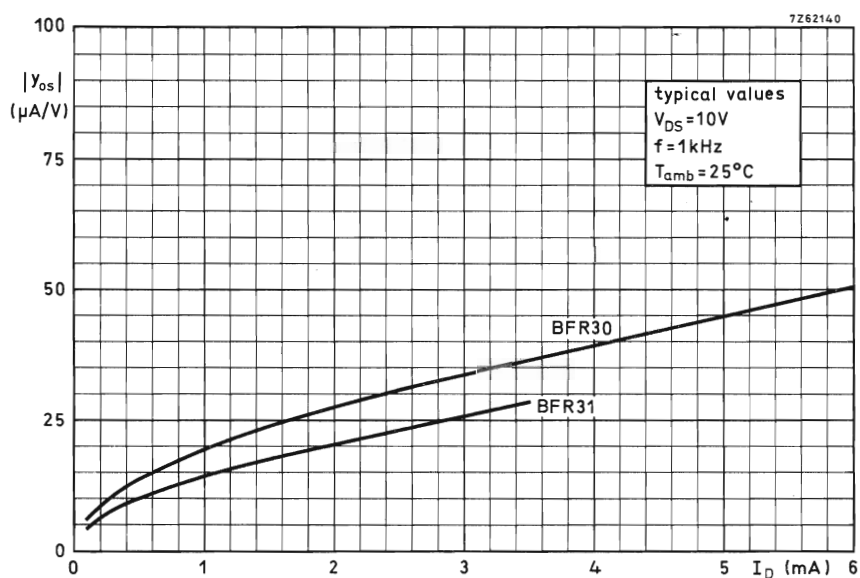


Fig. 11.

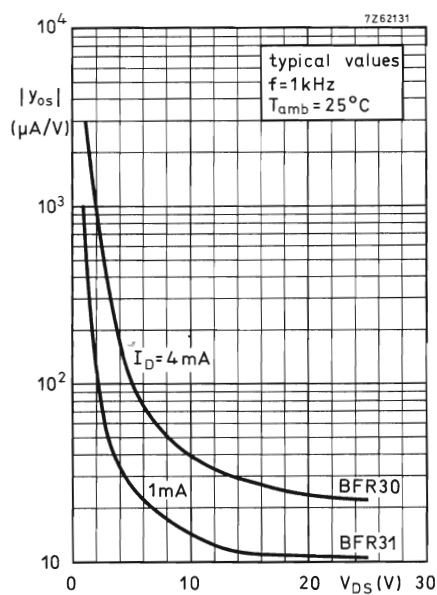


Fig. 12.

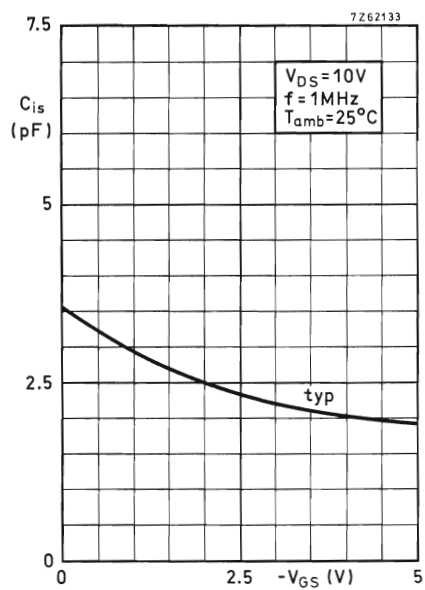


Fig. 13.

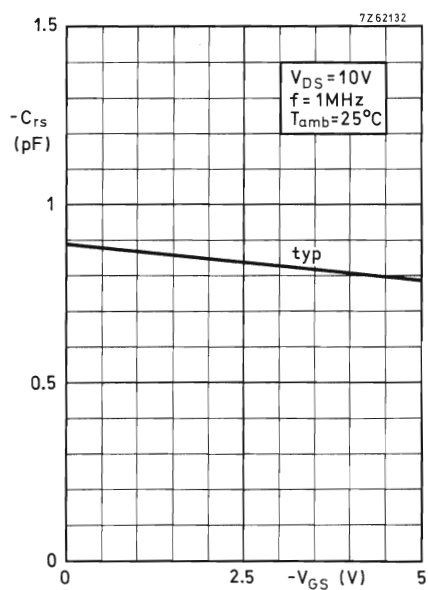


Fig. 14.

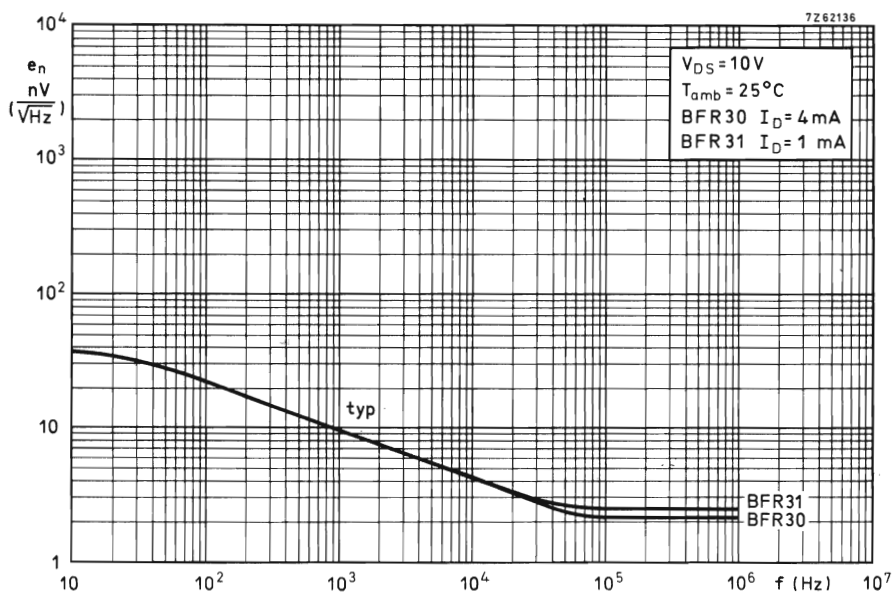


Fig. 15.

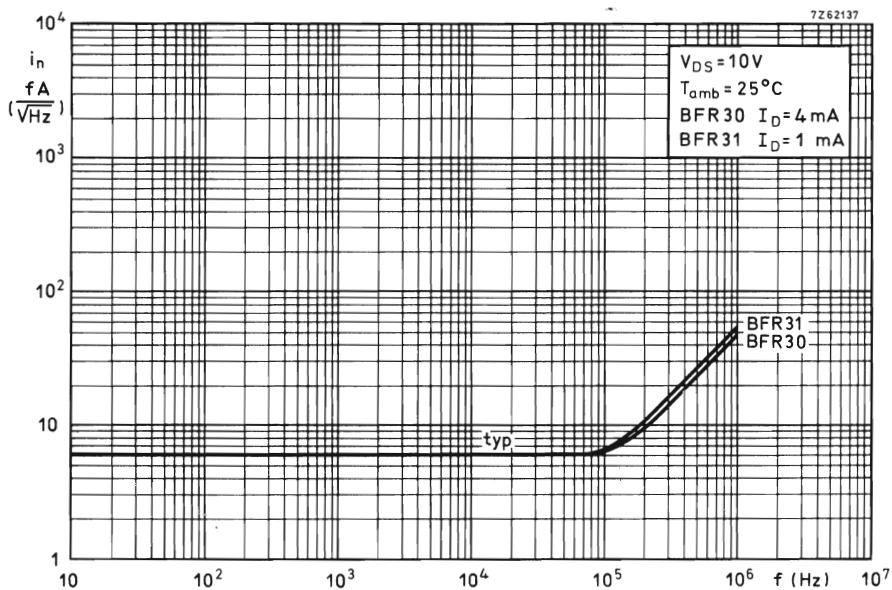


Fig. 16.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

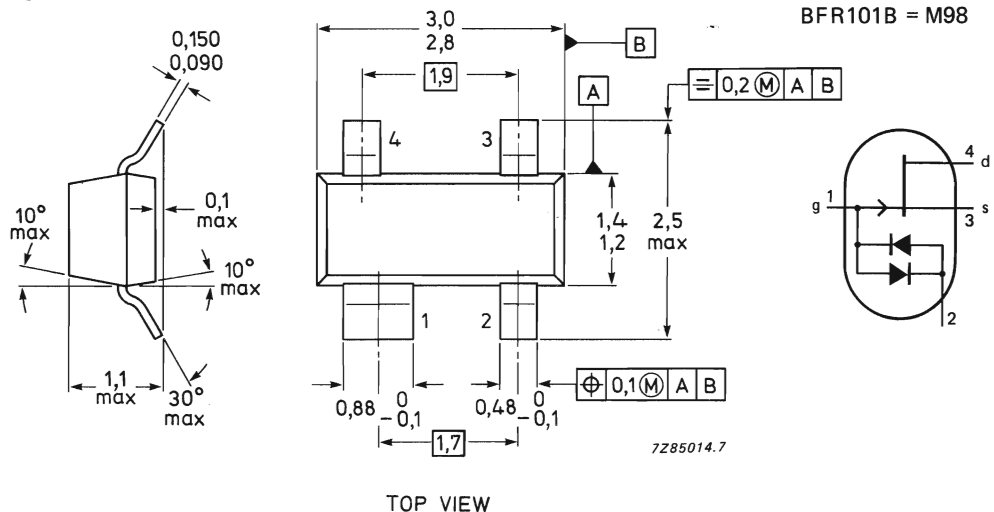
Symmetrical n-channel silicon junction field-effect transistor, designed primarily for use as a source follower with the input protected against successive voltage surges by a forward and reverse integrated diode.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Gate-source voltage (open drain)	$-V_{GS}$	max.	30 V
Total power dissipation up to $T_{amb} = 60^\circ\text{C}$	P_{tot}	max.	200 mW
Drain current			
$V_{DS} = 6\text{ V}; V_{GS} = 0$: BFR101A	I_{DSS}	0,2 to 1,5 mA	
$V_{DS} = 6\text{ V}; V_{GS} = 0$: BFR101B	I_{DSS}	1,0 to 5,0 mA	
Transfer admittance (common source)			
$V_{DS} = 6\text{ V}; V_{GS} = 0$; $f = 1\text{ kHz}$: BFR101A	$ y_{fs} $	>	1,2 mS
$V_{DS} = 6\text{ V}; V_{GS} = 0$; $f = 1\text{ kHz}$: BFR101B	$ y_{fs} $	>	2,5 mS

MECHANICAL DATA

Fig. 1 SOT-143.



Note: Drain and source are interchangeable.

See also *Soldering recommendations*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current (d.c.)	I_D	max.	20 mA
Gate current (d.c.)	I_G	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		-65 to + 150 $^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j-a}$	=	460 K/W
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CHARACTERISTICS with source connected to case for all measurements

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

		BFR101A	BFR101B
Gate leakage current $V_{DS} = 6\text{ V}; I_D = 10\text{ }\mu\text{A}$	$-I_G$	< 5	5 nA
Drain current* $V_{DS} = 6\text{ V}; V_{GS} = 0$	I_{DSS}	0,2 to 1,5	1 to 5 mA
Gate-source cut-off voltage $V_{DS} = 6\text{ V}; I_D = 1\text{ }\mu\text{A}$	$-V_{(P)GS}$	0,2 to 1	0,5 to 2,5 V
Small-signal common-source characteristics $V_{DS} = 6\text{ V}; V_{GS} = 0$			
Transfer admittance* $f = 1\text{ kHz}$	$ Y_{fs} $	> 1,2	2,5 mS
Output admittance at $f = 1\text{ kHz}^{**}$	$ Y_{os} $	typ. 10	50 mS
Input capacitance at $f = 1\text{ MHz}$ diodes not connected	C_{is}	< 5	5 pF
Diode capacitance $V_D = 0$; source and drain not connected	C_d	typ. 0,7	0,7 pF
Diode forward voltage $\pm I_F = 10\text{ mA}$	V_F	0,7 to 1,2	0,7 to 1,2 V

→ * Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

** Measured under pulse conditions: $t_p = 100\text{ ms}$; $\delta \leq 0,1$.

MATCHED N-CHANNEL FETS

Matched pair of symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes, mounted together in a metal S-clip.

These devices are intended for low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at $T_{amb} = 25^{\circ}\text{C}$; $I_D = 0,5\text{ mA}$; $V_{DG} = 15\text{ V}$

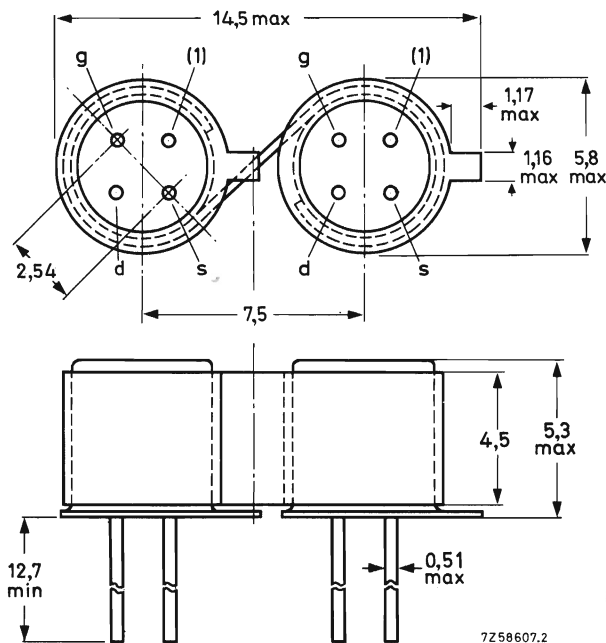
		BFS21	BFS21A
Gate cut-off current	I_G	< 0,5	0,5 nA
Gate -source voltage difference	$ \Delta V_{GS} $	< 20	10 mV
Thermal drift of gate-source voltage difference	$\left \frac{d\Delta V_{GS}}{dT} \right $	< 75	40 $\mu\text{V/K}$
Difference in transfer impedance	$\left \Delta \frac{1}{g_{fs}} \right $	< 15	7,5 Ω
Difference in penetration factor	$\left \Delta \frac{g_{os}}{g_{fs}} \right $	< 1	0,5 mV/V
Common mode rejection ratio	CMRR	> 60	66 dB

MECHANICAL DATA

SOT-52 (see next page)

TOTAL DEVICE
MECHANICAL DATA
SOT-52

Dimensions in mm



(1) = shield lead (connected to case).

Maximum lead diameter is guaranteed only for 12,7 mm.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage between any 2 terminals	V	max.	30 V
Drain current	I_D	max.	4 mA
Gate current	I_G	max.	0,5 mA
Total power dissipation up to $T_{amb} = 100\text{ }^{\circ}\text{C}$	P_{tot}	max.	30 mW
Operating ambient temperature	T_{amb}		-20 to + 100 $^{\circ}\text{C}$

CHARACTERISTICS (total device) $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

		BFS21	BFS21A
Drain current ratio			
$V_{DG} = 15\text{ V}; V_{GS} = 0; T_j = 25\text{ }^{\circ}\text{C}$	$\frac{I_{D1-S1S}}{I_{D2-S2S}}$	$> 0,95$	0,95
		$< 1,05$	1,05
Gate-source voltage difference			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$ \Delta V_{GS} $	< 20	10 mV
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$ \Delta V_{GS} $	< 20	10 mV
Thermal drift of gate-source voltage difference			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left \frac{d \Delta V_{GS}}{dT} \right $	< 75	40 $\mu\text{V/K}$
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left \frac{d \Delta V_{GS}}{dT} \right $	< 75	40 $\mu\text{V/K}$
Change of gate-source voltage difference with ambient temperature			
$T_{amb} = 25\text{ to }100\text{ }^{\circ}\text{C}$			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$ \Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1}) $	< 6	3 mV
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$ \Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1}) $	< 6	3 mV
Difference of penetration factors ¹⁾			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left \Delta \frac{g_{os}}{g_{fs}} \right $	< 1	0,5 10^{-3}
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left \Delta \frac{g_{os}}{g_{fs}} \right $	< 1	0,5 10^{-3}
Difference of transfer impedances ²⁾			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left \Delta \frac{1}{g_{fs}} \right $	< 15	7,8 Ω
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left \Delta \frac{1}{g_{fs}} \right $	< 75	37,5 Ω

- 1) The difference between the penetration factors is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$$\left(\Delta \frac{g_{os}}{g_{fs}} = \frac{d \Delta V_{GS}}{d V_{DG}} \text{ at } I_D = \text{constant} \right)$$

- 2) The difference between the transfer impedances is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$$\left(\Delta \frac{1}{g_{fs}} = \frac{d \Delta V_{GS}}{d I_D} \text{ at } V_{DG} = \text{constant} \right)$$

CHARACTERISTICS (continued) (total device)

Common mode rejection ratio ¹⁾

$$I_D = 500 \mu A; V_{DG} = 15 V$$

$$I_D = 100 \mu A; V_{DG} = 15 V$$

	BFS21	BFS21A
CMRR	> 60	66 dB
CMRR	> 60	66 dB

INDIVIDUAL TRANSISTOR

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	I_D	max.	20 mA
Gate current	I_G	max.	10 mA
Total power dissipation up to $T_{amb} = 25^\circ$	P_{tot}	max.	300 mW
Storage temperature	T_{stg}	-65 to +200	$^\circ C$
Junction temperature	T_j	max.	200 $^\circ C$

THERMAL RESISTANCE

From junction to ambient in free air
(for individual transistor without S-clip)

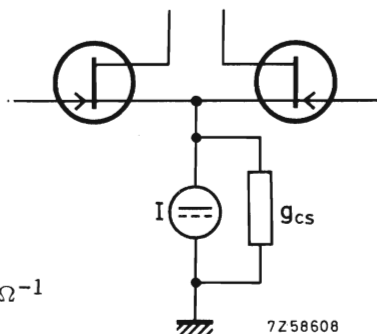
$$R_{th j-a} = 590 K/W$$

¹⁾ Common mode rejection ratio

$$(CMRR)^{-1} = \Delta \frac{g_{os}}{g_{fs}} + \frac{1}{2} g_{cs} \Delta \frac{1}{g_{fs}}$$

where g_{cs} in this formula is the output conductance of the summing current source.

The guaranteed values of CMRR apply at $g_{cs} = 0.1 \mu\Omega^{-1}$



CHARACTERISTICS (individual transistor) $T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified

Gate cut-off current

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}$

$I_G < 0,5 \text{ nA}$

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}; T_{amb} = 100^{\circ}\text{C}$

$I_G < 25 \text{ nA}$

Drain current

$V_{DS} = 15 \text{ V}, V_{GS} = 0, T_j = 25^{\circ}\text{C}$

$I_{DSS} > 1 \text{ mA}$

Gate-source cut-off voltage

$I_D = 0,5 \text{ nA}, V_{DS} = 15 \text{ V}$

$-V_{(P)GS} < 6 \text{ V}$

Transfer conductance at $f = 1 \text{ kHz}$

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}$

$g_{fs} > 1,0 \text{ mS}$

Output conductance at $f = 1 \text{ kHz}$

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}$

$g_{os} < 15 \mu\text{S}$

Input capacitance at $f = 1 \text{ MHz}$

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}$

$C_{is} < 5 \text{ pF}$

Feedback capacitance at $f = 1 \text{ MHz}$

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}$

$C_{rs} < 0,75 \text{ pF}$

Equivalent noise voltage

$f = 10 \text{ Hz}$

$I_D = 500 \mu\text{A}; V_{DS} = 15 \text{ V}$

$V_n/\sqrt{B} < 200 \text{ nV}/\sqrt{\text{Hz}}$

$V_{DS} = 15 \text{ V}, V_{GS} = 0$

$V_n/\sqrt{B} < 75 \text{ nV}/\sqrt{\text{Hz}}$

N-CHANNEL SILICON FET

Symmetrical n-channel silicon epitaxial planar junction field-effect transistor in a microminiature plastic envelope. The transistor is intended for low level general purpose amplifiers in thick and thin-film circuits.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Total power dissipation up to $T_{amb} = 65^\circ\text{C}$	P_{tot}	max.	250 mW
Drain current			
$V_{DS} = 10\text{ V}; V_{GS} = 0$	I_{DSS}	>	0,2 mA
		<	1,5 mA
Transfer admittance (common source)			
$I_D = 0,2\text{ mA}; V_{DS} = 10\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	>	0,5 mS
Equivalent noise voltage			
$V_{DS} = 10\text{ V}; I_D = 200\text{ }\mu\text{A}; B = 0,6\text{ to }100\text{ Hz}$	V_n	<	0,5 μV

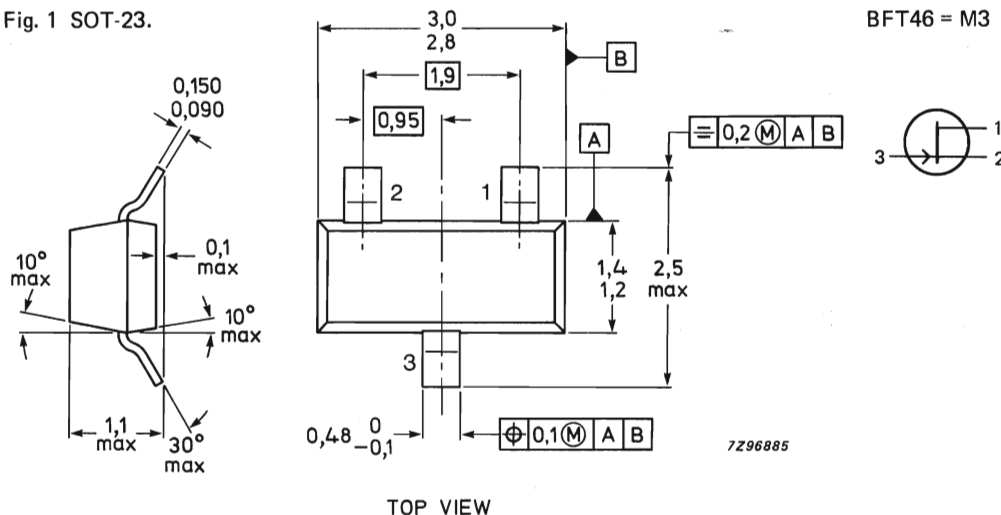
MECHANICAL DATA

Dimensions in mm

Marking code

Fig. 1 SOT-23.

BFT46 = M3



Note : Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Drain-gate voltage (open source)	V_{DGO}	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Drain current	I_D	max.	10 mA
Gate current	I_G	max.	5 mA
Total power dissipation up to $T_{amb} = 65\text{ }^{\circ}\text{C}^{**}$	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		-65 to +175 $^{\circ}\text{C}$
Junction temperature	T_j	max.	175 $^{\circ}\text{C}$

THERMAL CHARACTERISTICS*

$$R_{th\ j-t} + R_{th\ t-s} + R_{th\ s-a} = \frac{T_j - T_{amb}}{P}$$

Thermal resistance

From junction to tab	$R_{th\ j-t}$	=	60 K/W
From tab to soldering points	$R_{th\ t-s}$	=	280 K/W
From soldering points to ambient**	$R_{th\ s-a}$	=	90 K/W

CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off current

$-V_{GS} = 10\text{ V}; V_{DS} = 0$

$-I_{GSS} < 0,2\text{ nA}$

Drain current **

$V_{DS} = 10\text{ V}; V_{GS} = 0$

$$I_{DSS} > 0,2\text{ mA}$$

$$< 1,5\text{ mA}$$

Gate-source voltage

$I_D = 50\text{ }\mu\text{A}; V_{DS} = 10\text{ V}$

$$-V_{GS} > 0,1\text{ V}$$

$$< 1,0\text{ V}$$

Gate-source cut-off voltage

$I_D = 0,5\text{ nA}; V_{DS} = 10\text{ V}$

$-V_{(P)GS} < 1,2\text{ V}$

y-parameters at $f = 1\text{ kHz}$;

$V_{DS} = 10\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^{\circ}\text{C}$

Transfer admittance

$|y_{fs}| > 1,0\text{ mS}$

Output admittance

$|y_{os}| < 10\text{ }\mu\text{S}$

$V_{DS} = 10\text{ V}; I_D = 200\text{ }\mu\text{A};$

Transfer admittance

$|y_{fs}| > 0,5\text{ mS}$

Output admittance

$|y_{os}| < 5\text{ }\mu\text{S}$

* See *Thermal characteristics*.

** Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Input capacitance at $f = 1 \text{ MHz}$;

$V_{DS} = 10 \text{ V}$; $V_{GS} = 0$; $T_{amb} = 25^\circ\text{C}$

$C_{is} < 5 \text{ pF}$

Feedback capacitance at $f = 1 \text{ MHz}$;

$V_{DS} = 10 \text{ V}$; $V_{GS} = 0$; $T_{amb} = 25^\circ\text{C}$

$C_{rs} < 1,5 \text{ pF}$

Equivalent noise voltage

$V_{DS} = 10 \text{ V}$; $I_D = 200 \mu\text{A}$; $T_{amb} = 25^\circ\text{C}$

$B = 0,6 \text{ to } 100 \text{ Hz}$

$V_n < 0,5 \mu\text{V}$

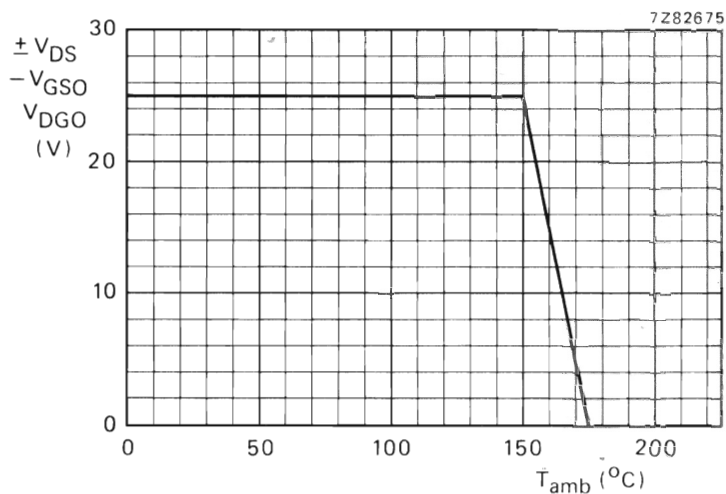


Fig. 2 Voltage derating curve.

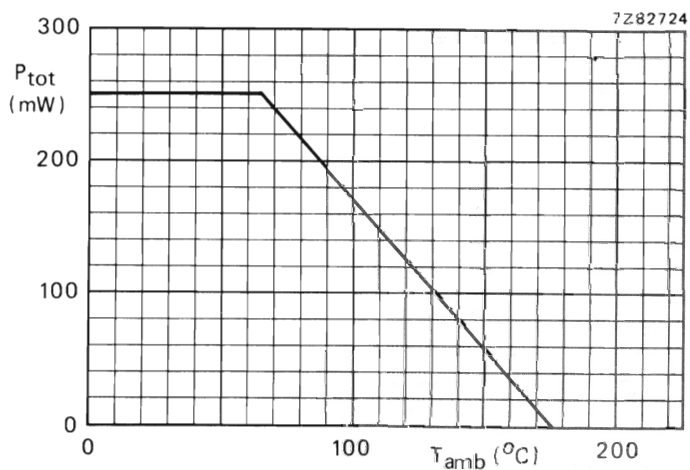
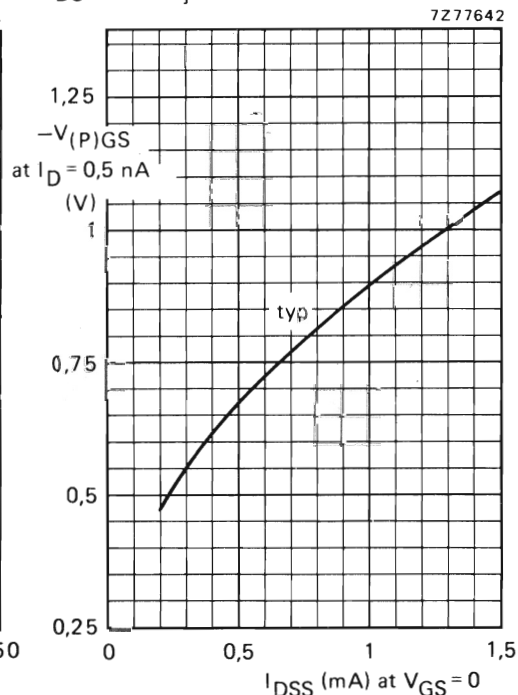
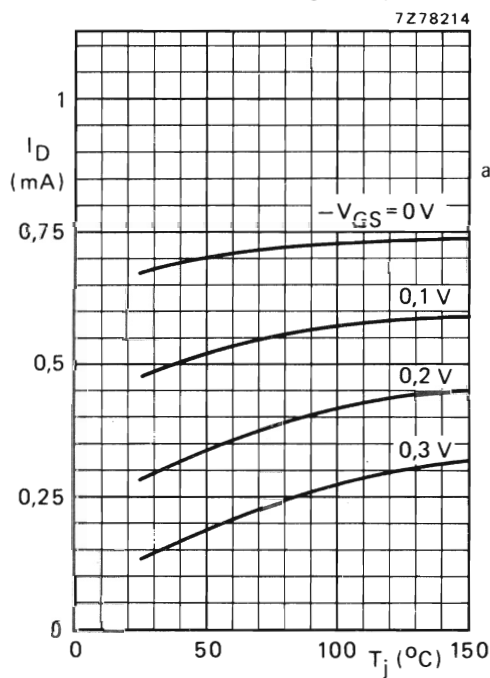
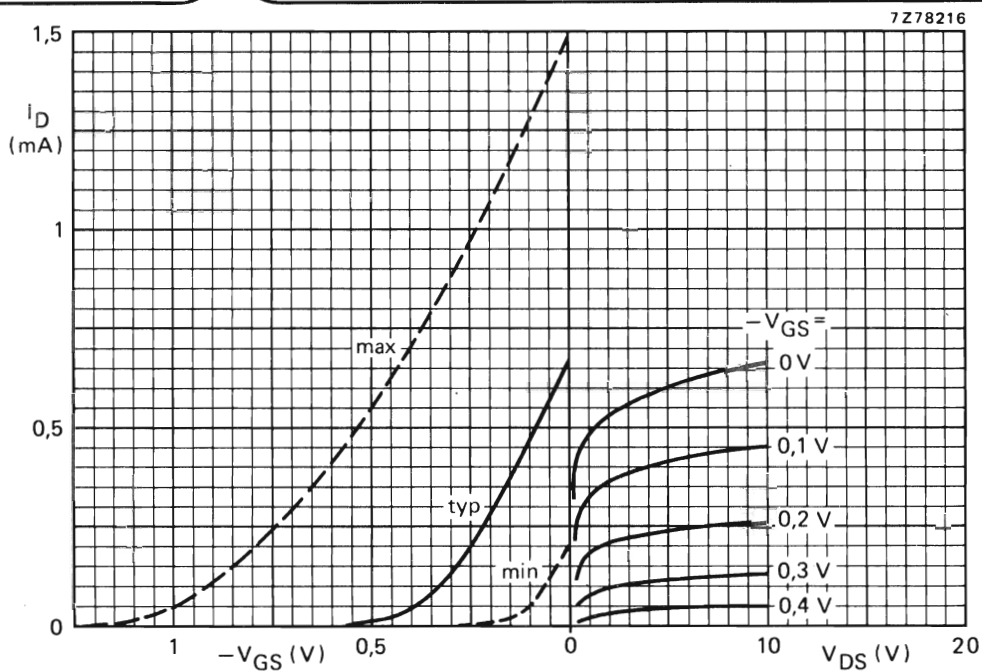


Fig. 3 Power derating curve.



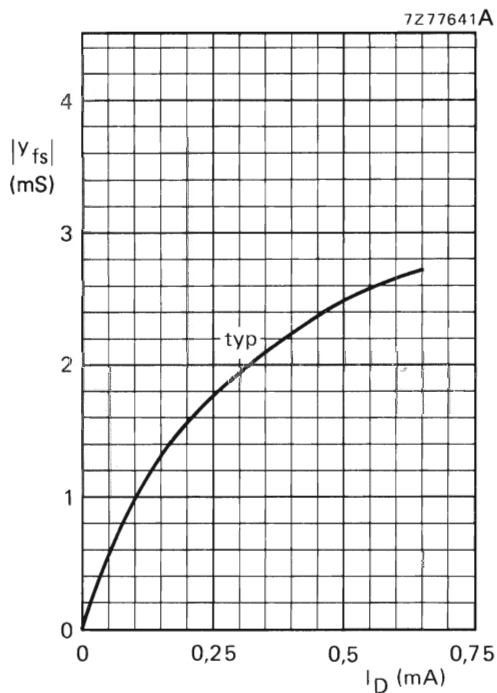


Fig. 7.

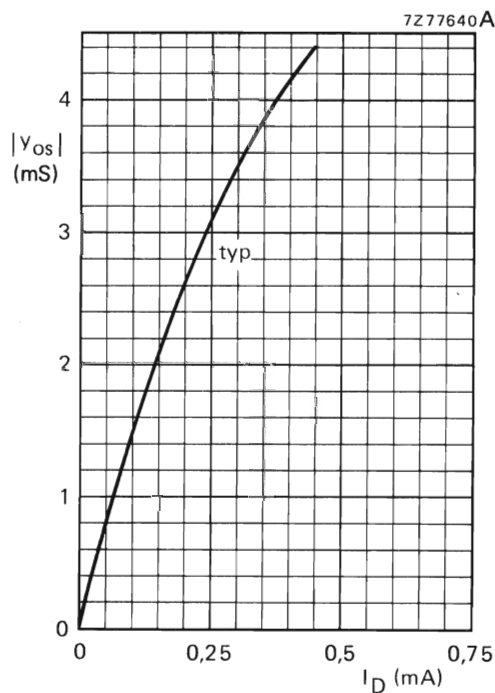


Fig. 8.

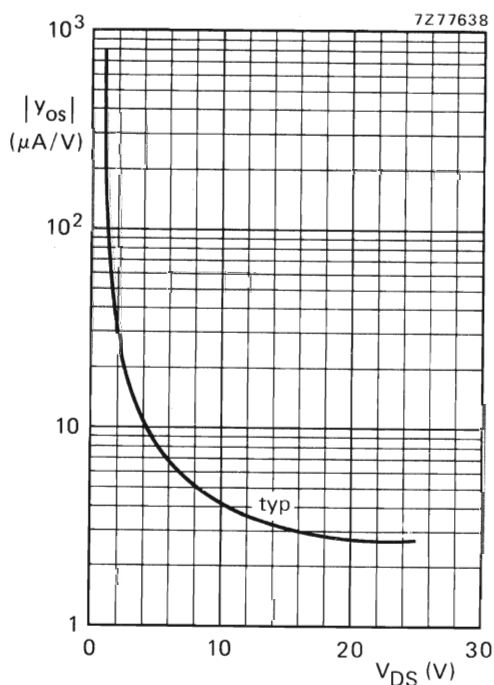


Fig. 9.

Fig. 7 $|y_{fs}|$ versus I_D .
 $V_{DS} = 10 \text{ V}$; $f = 1 \text{ kHz}$; $T_{amb} = 25^\circ \text{C}$.

Fig. 8 $|y_{os}|$ versus I_D .
 $V_{DS} = 10 \text{ V}$; $f = 1 \text{ kHz}$; $T_{amb} = 25^\circ \text{C}$.

Fig. 9 $|y_{os}|$ versus V_{DS} .
 $I_D = 0.4 \text{ mA}$; $f = 1 \text{ kHz}$; $T_{amb} = 25^\circ \text{C}$.

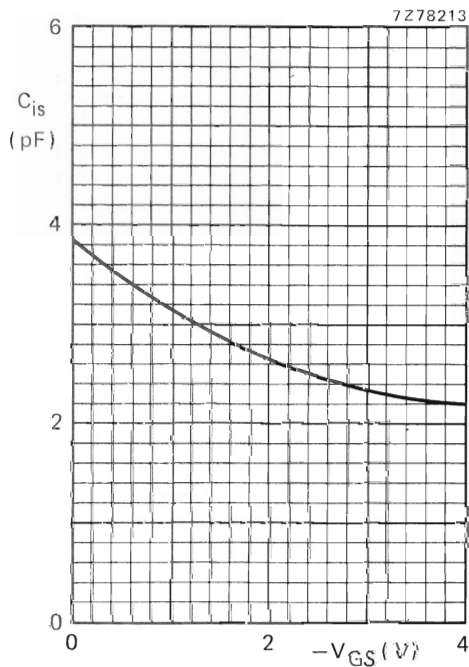


Fig. 10.

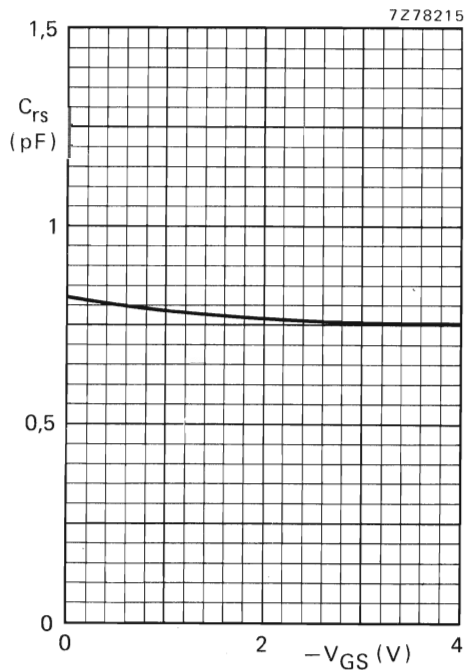


Fig. 11.

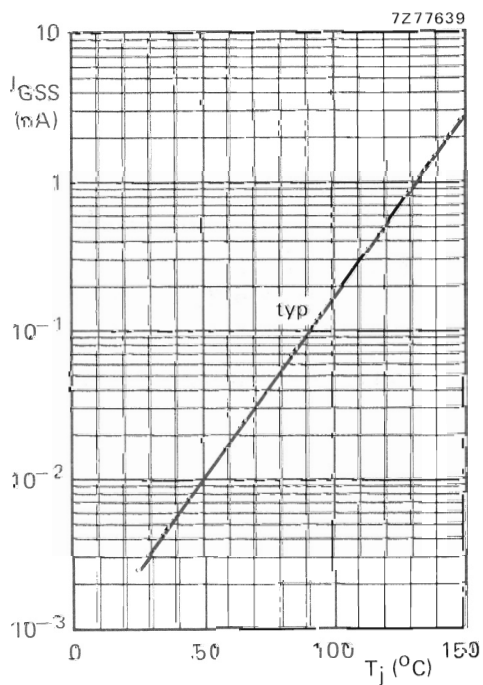
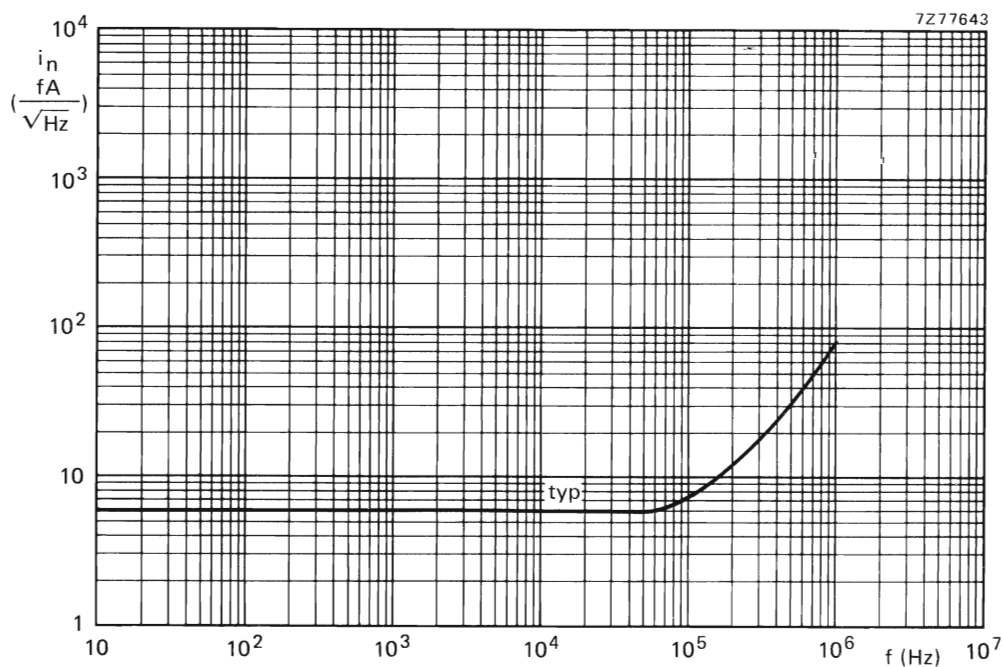
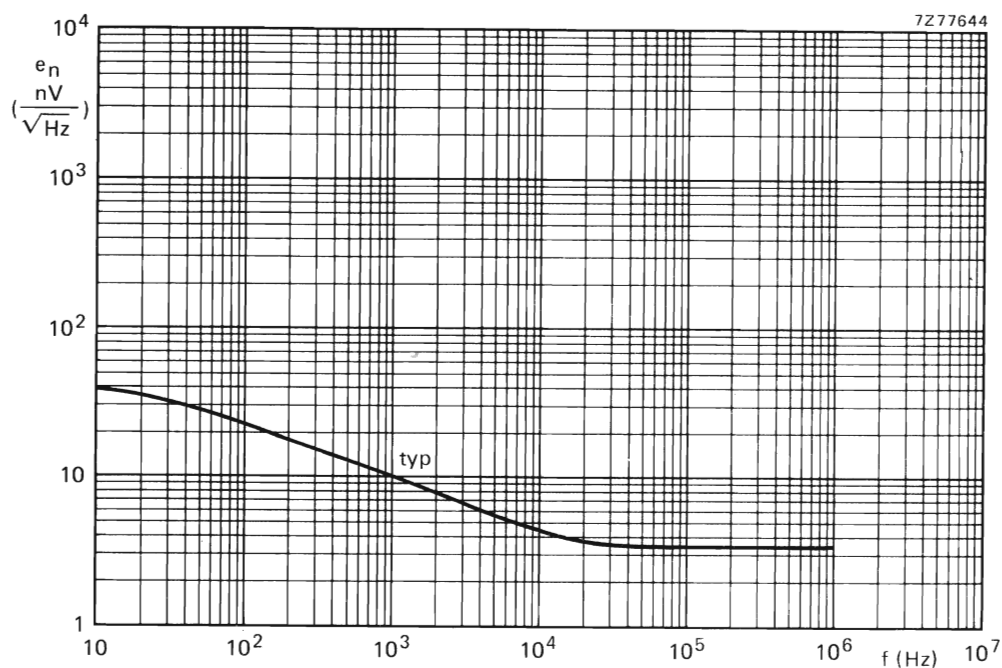


Fig. 12.

Fig.10 Typical values.
 $V_{DS} = 10$ V, $T_{amb} = 25$ °C.

Fig.11 Typical values.
 $V_{DS} = 10$ V, $T_{amb} = 25$ °C.

Fig.12 I_{GSS} versus T_j .
 $-V_{GS} = 10$ V; $V_{DS} = 0$.



N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are designed for broad band amplifiers (0 to 300 MHz). Their very low noise at low frequencies makes these devices very suitable for differential amplifiers, electro-medical and nuclear detector preamplifiers.

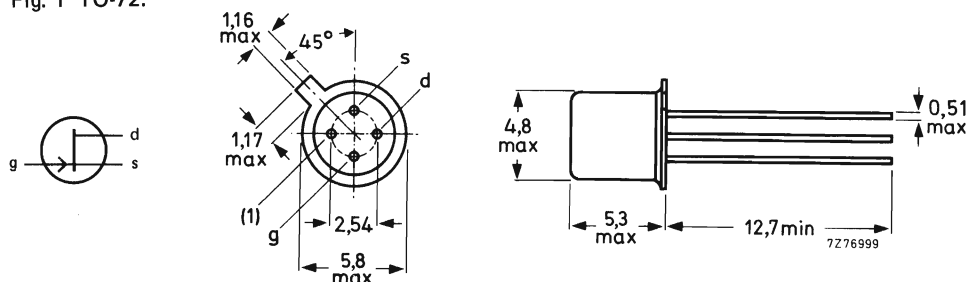
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V	
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V	
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300	mW	
			BFW10	BFW11	
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}	$>$	8	4	mA
		$<$	20	10	mA
Gate-source cut-off voltage $I_D = 0,5\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	$<$	8	6	V
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 15\text{ V}; V_{GS} = 0$	C_{rs}	$<$	0,80	0,80	pF
Transfer admittance (common source) $V_{DS} = 15\text{ V}; V_{GS} = 0; f = 200\text{ MHz}$	$ y_{fs} $	$>$	3,2	3,2	mS
Noise figure at $V_{DS} = 15\text{ V}; V_{GS} = 0$ $f = 100\text{ MHz}; R_G = 1\text{ k}\Omega$	F	$<$	2,5	2,5	dB
Equivalent noise voltage $f = 10\text{ Hz}$	V_n/\sqrt{B}	$<$	75	75	nV/ $\sqrt{\text{Hz}}$

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



Note: Drain and source are interchangeable.

(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	I_D	max.	20 mA
Gate current	I_G	max.	10 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
Storage temperature	T_{stg}	-65 to +200 $^{\circ}\text{C}$	
Junction temperature	T_j	max.	200 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	590 K/W
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CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

$-V_{GS} = 20\text{ V}; V_{DS} = 0$

		BFW10	BFW11
$-I_{GSS}$	<	0.1	0.1 nA

$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_j = 150\text{ }^{\circ}\text{C}$

$-I_{GSS}$	<	0.5	0.5 μA
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Drain current ¹⁾

$V_{DS} = 15\text{ V}; V_{GS} = 0$

I_{DSS}	>	8	4 mA
	<	20	10 mA

Gate-source voltage

$I_D = 400\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$

$-V_{GS}$	>	2.0	V
	<	7.5	V

$I_D = 50\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$

$-V_{GS}$	>	1.25	V
	<	4.0	V

Gate-source cut-off voltage

$I_D = 0.5\text{ nA}; V_{DS} = 15\text{ V}$

$-V_{(P)GS}$	<	8	6 V
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y parameters

$V_{DS} = 15\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^{\circ}\text{C}$

$f = 1\text{ kHz}$ Transfer admittance

$ y_{fs} $	>	3.5	3.0 mS
	<	6.5	6.5 mS

Output admittance

$ y_{os} $	<	85	50 μS
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$f = 1\text{ MHz}$ Input capacitance

C_{is}	typ.	4	4 pF
	<	5	5 pF

Feedback capacitance

$-C_{rs}$	typ.	0.6	0.6 pF
	<	0.80	0.80 pF

$f = 200\text{ MHz}$ Transfer admittance

$ y_{fs} $	>	3.2	3.2 mS
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Input conductance

g_{is}	<	800	800 μS
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Output conductance

g_{os}	<	200	100 μS
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Noise figure at $f = 100\text{ MHz}$; $R_G = 1\text{ k}\Omega$

$V_{DS} = 15\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^{\circ}\text{C}$
input tuned to minimum noise

F	<	2.5	2.5 dB
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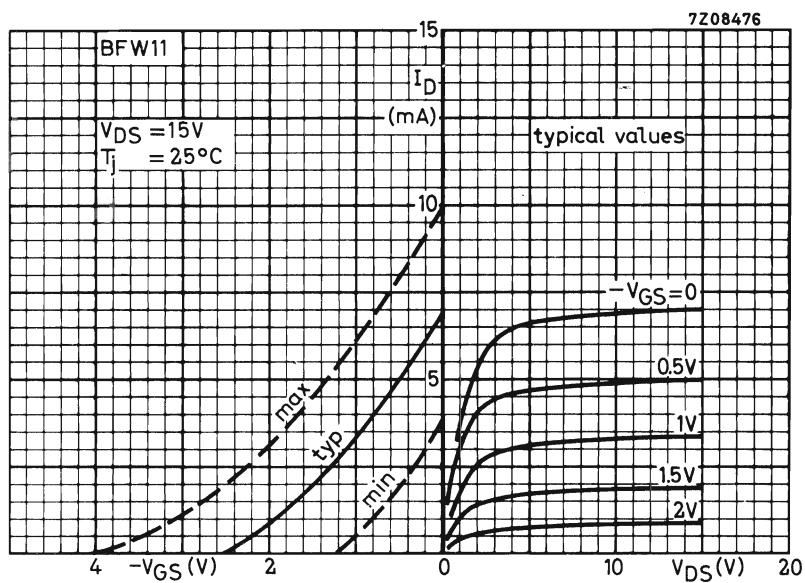
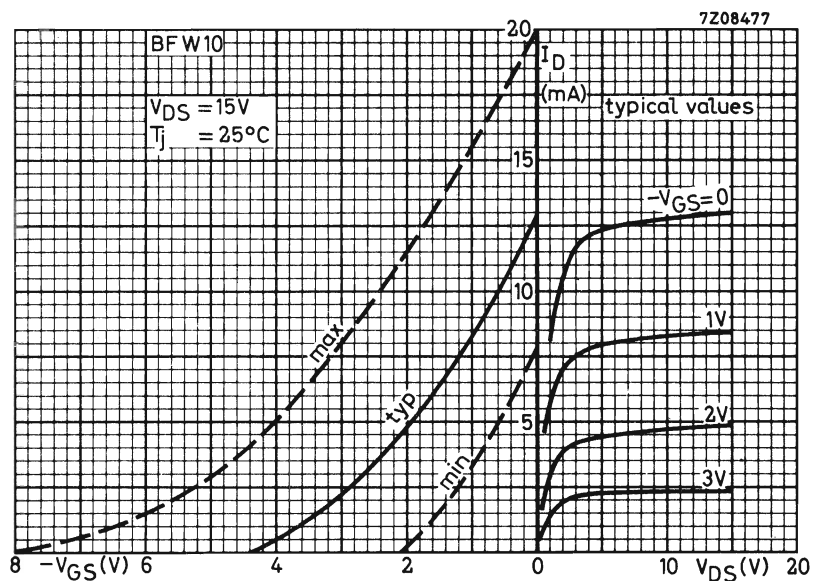
Equivalent noise voltage

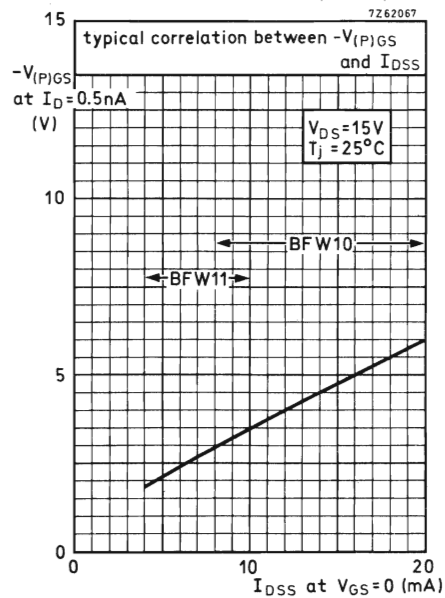
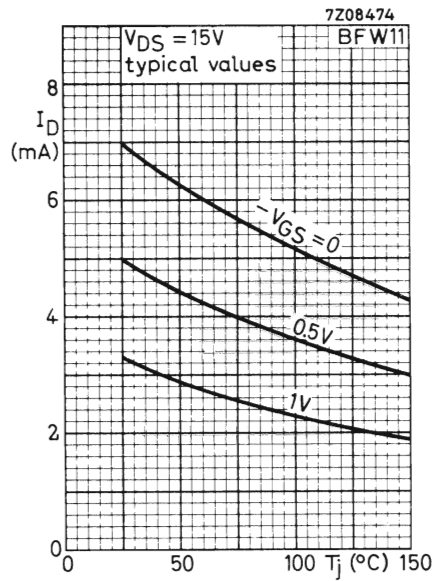
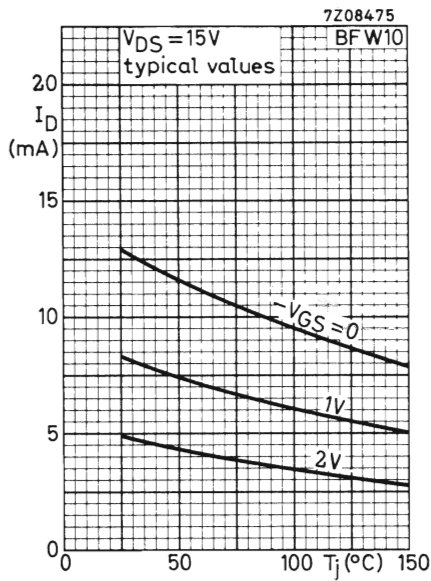
$V_{DS} = 15\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^{\circ}\text{C}$

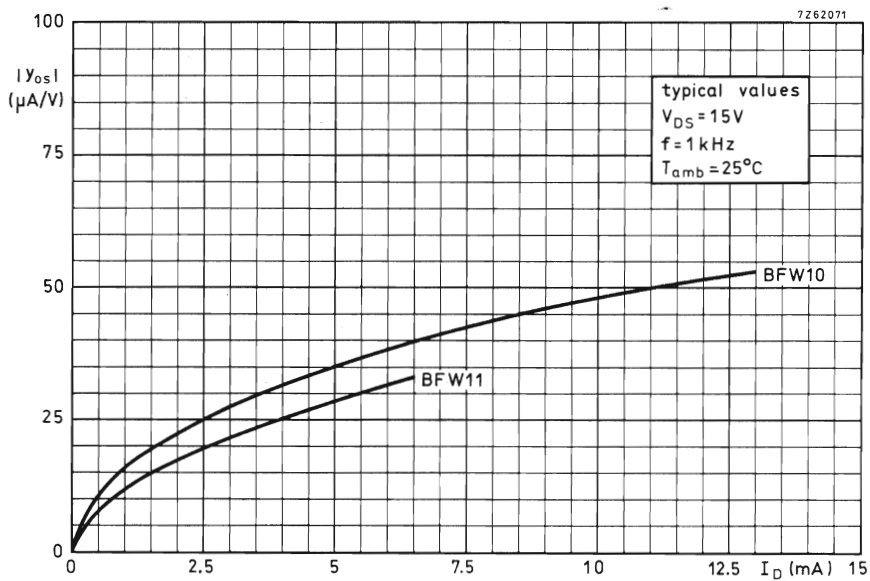
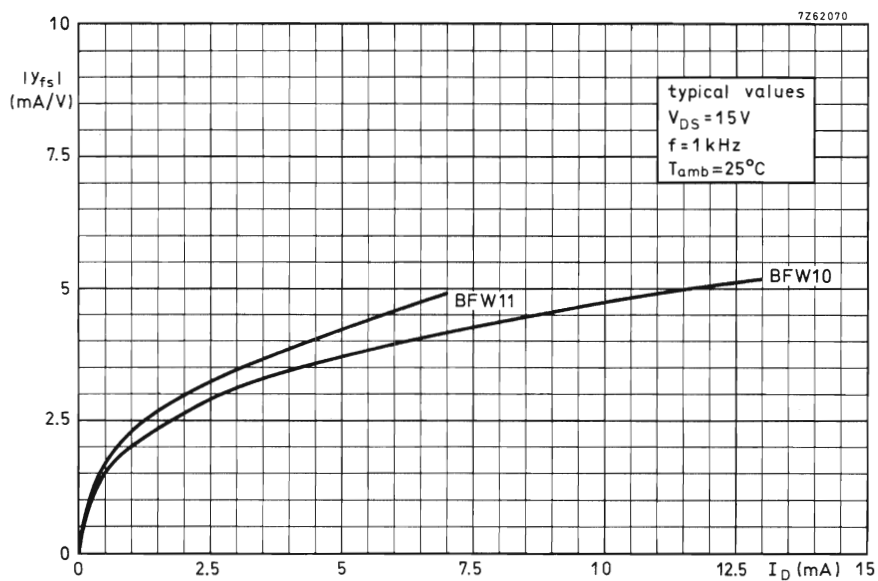
$f = 10\text{ Hz}$

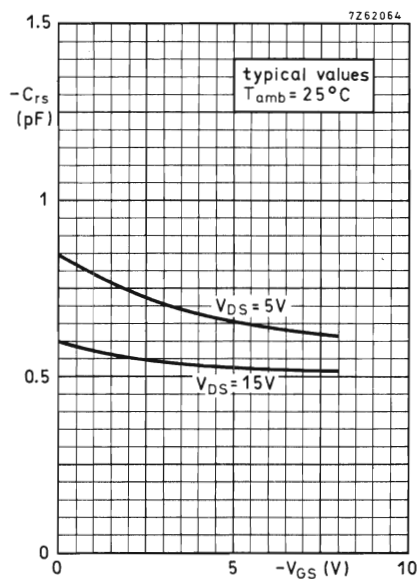
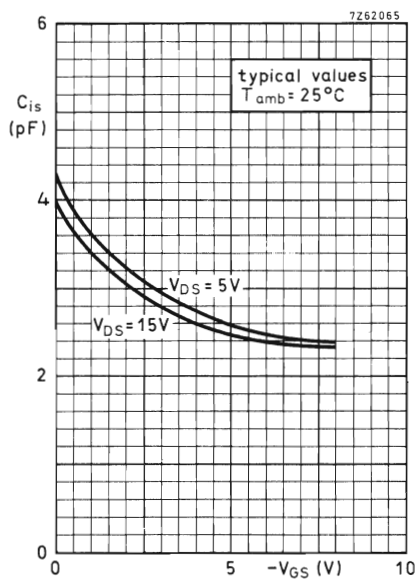
V_n/\sqrt{B}	<	75	75 nV/ $\sqrt{\text{Hz}}$
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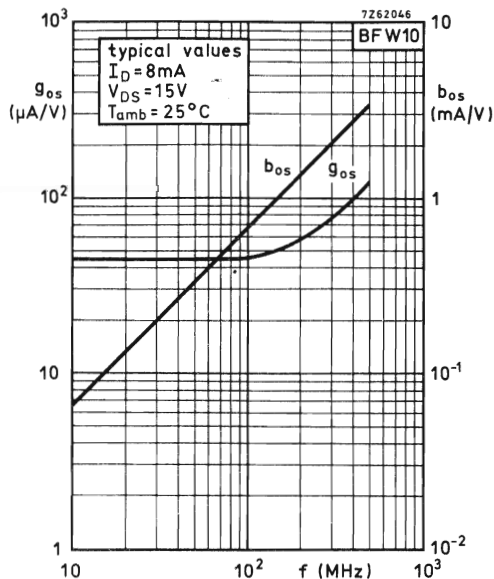
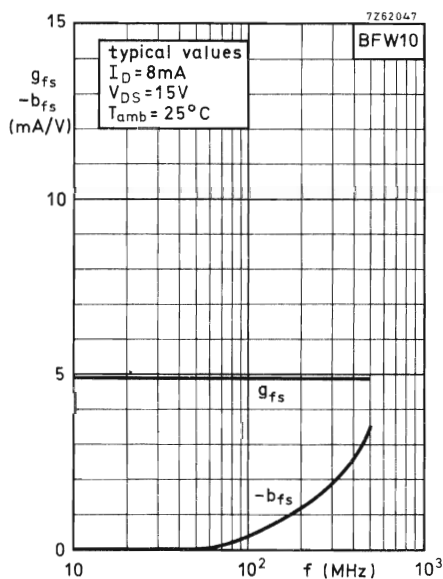
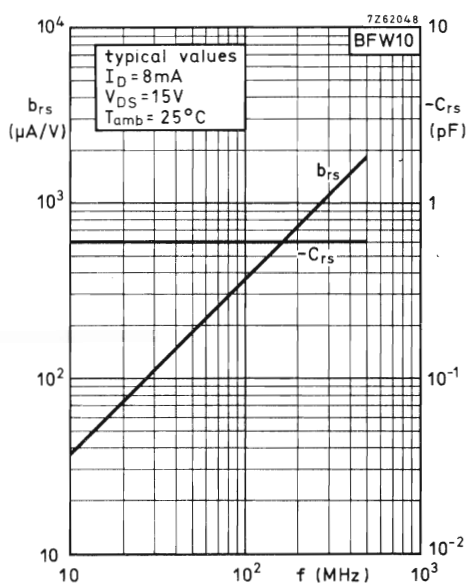
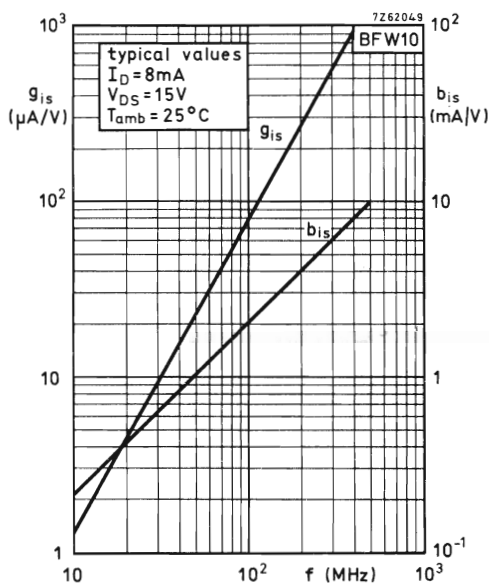
¹⁾ Measured under pulsed conditions.

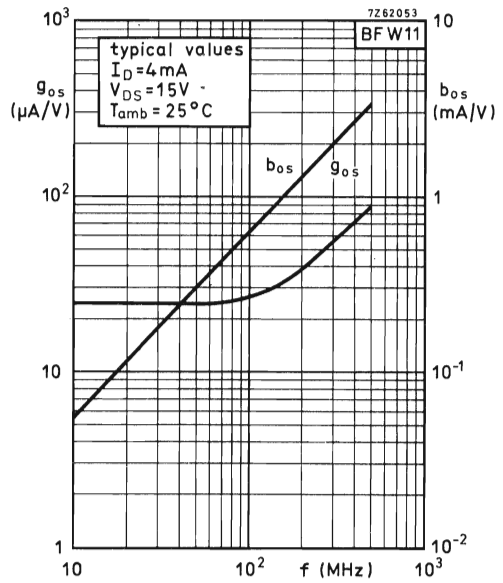
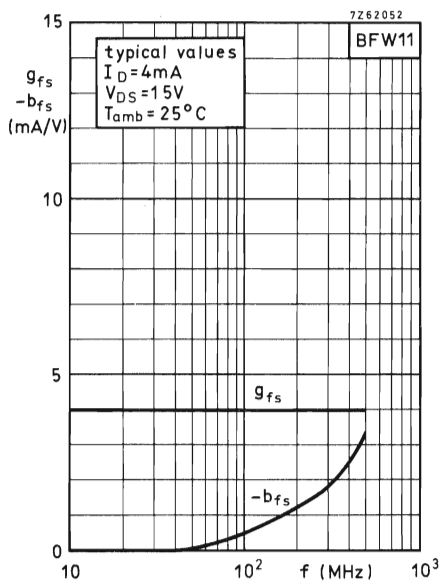
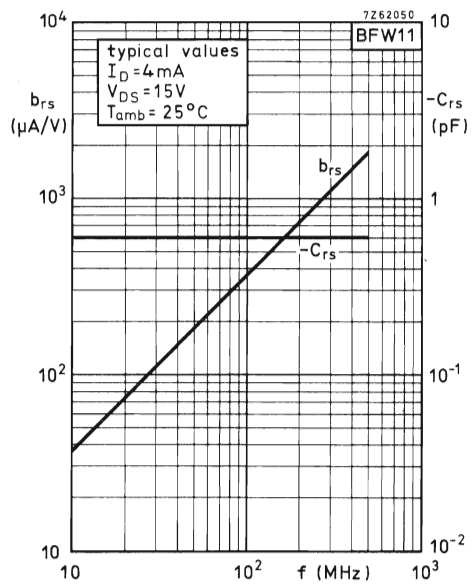
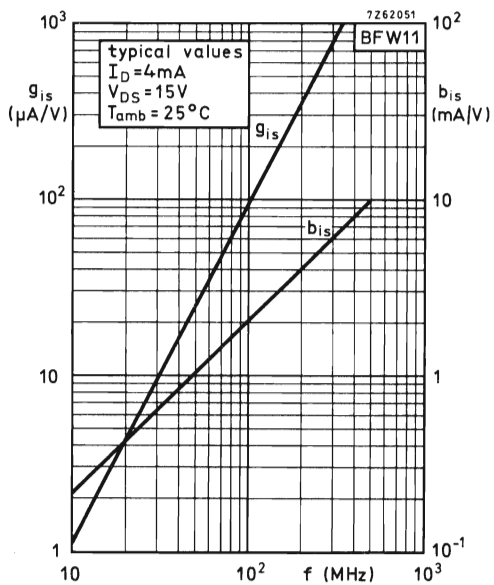


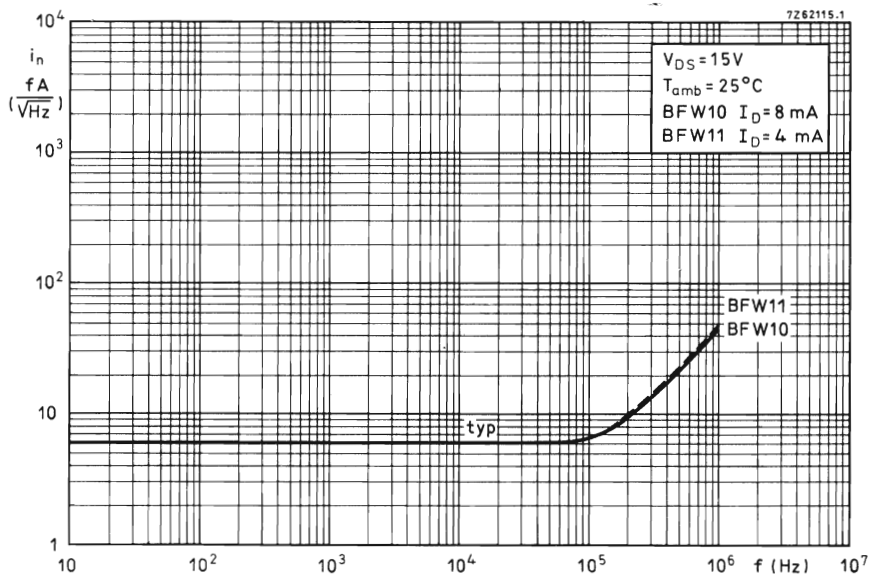
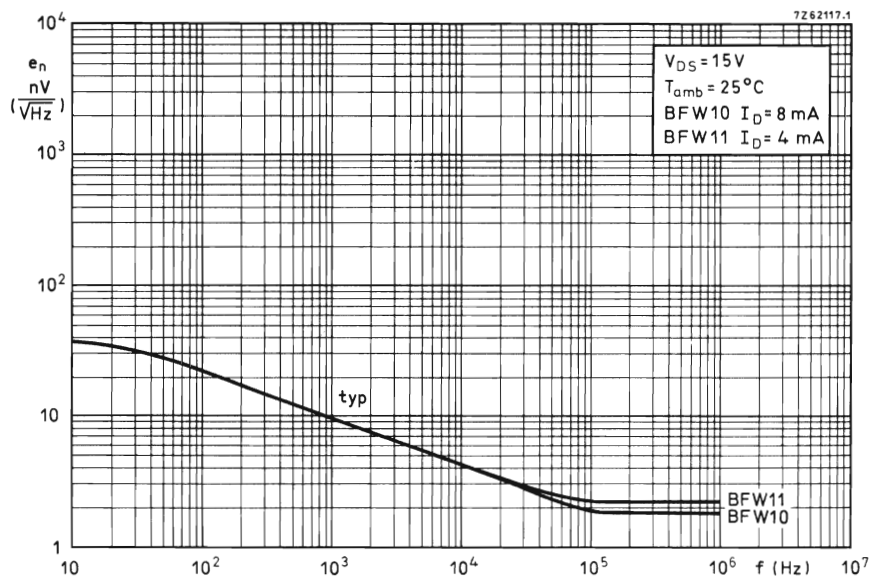


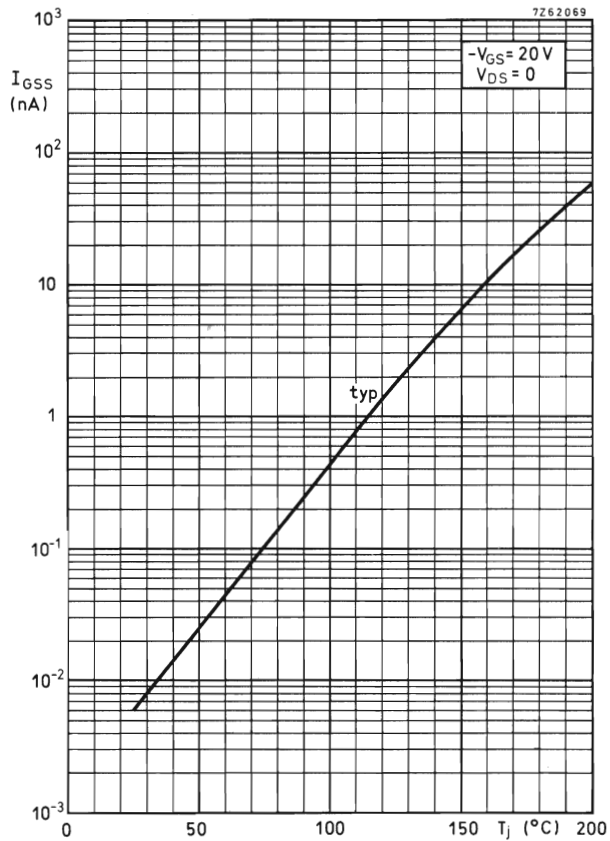












N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are intended for battery powered equipment and other low current-low voltage applications.

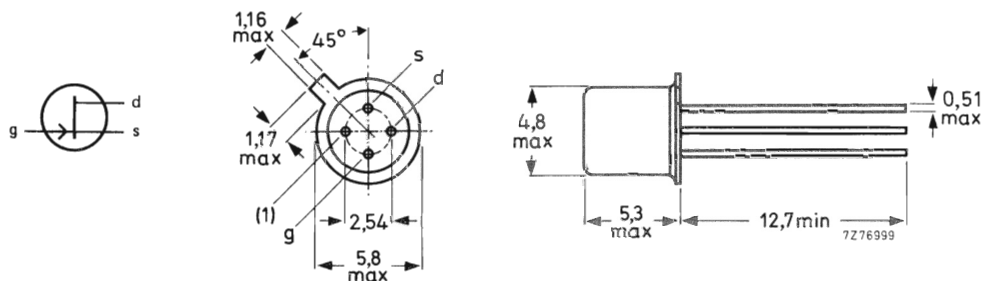
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V	
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V	
Total power dissipation up to $T_{amb} = 110\text{ }^{\circ}\text{C}$	P_{tot}	max.	150	mW	
			BFW12	BFW13	
Drain current					
$V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}	$>$	1	0,2	mA
		$<$	5	1,5	mA
Gate-source cut-off voltage					
$I_D = 0,5\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	$<$	2,5	1,2	V
Feedback capacitance at $f = 1\text{ MHz}$					
$V_{DS} = 15\text{ V}; V_{GS} = 0$	C_{rs}	$<$	0,80	0,80	pF
Transfer admittance (common source)					
$V_{DS} = 15\text{ V}; I_D = 200\text{ }\mu\text{A}; f = 1\text{ kHz}$	$ y_{fs} $	$>$	0,5	0,5	mS
Equivalent noise voltage					
$V_{DS} = 15\text{ V}; I_D = 200\text{ }\mu\text{A}$	V_n	$<$	0,5	0,5	μV
$B = 0,6\text{ to }100\text{ Hz}$					

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



Note: Drain and source are interchangeable.

(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	I_D	max.	10 mA
Gate current	I_G	max.	5 mA
Total power dissipation up to $T_{amb} = 110\text{ }^{\circ}\text{C}$	P_{tot}	max.	150 mW
Storage temperature	T_{stg}	-65 to +200	$^{\circ}\text{C}$
Junction temperature	T_j	max.	200 $^{\circ}\text{C}$

THERMAL RESISTANCE

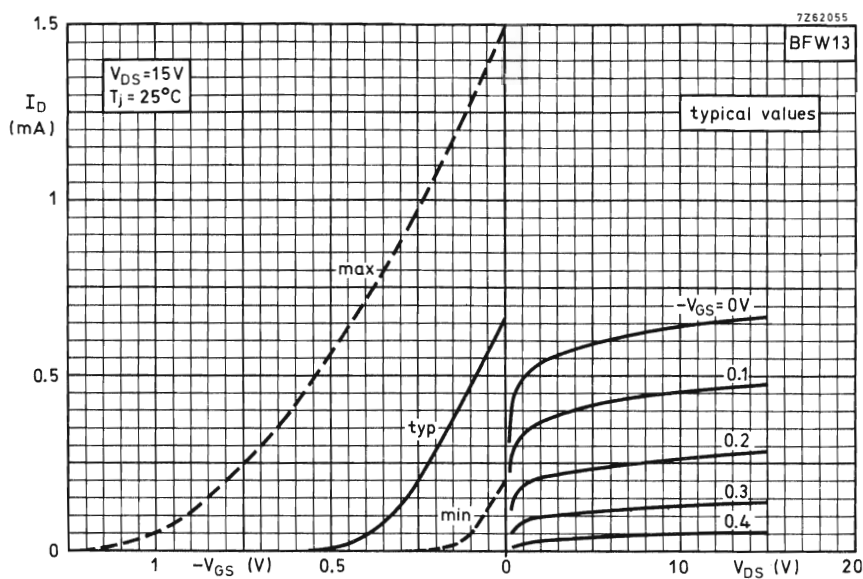
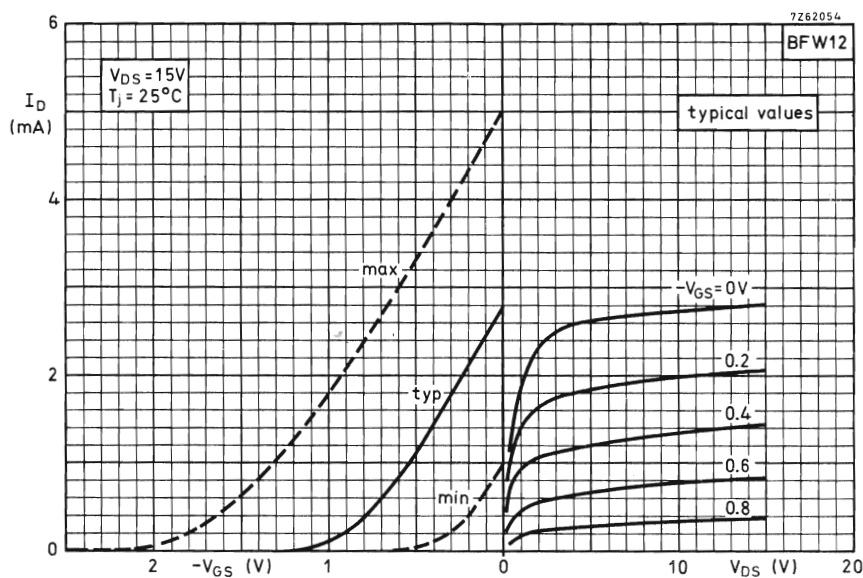
From junction to ambient	$R_{th\ j-a}$	=	590 K/W
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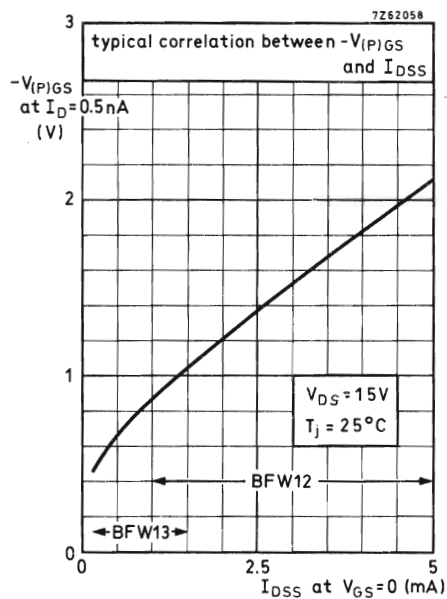
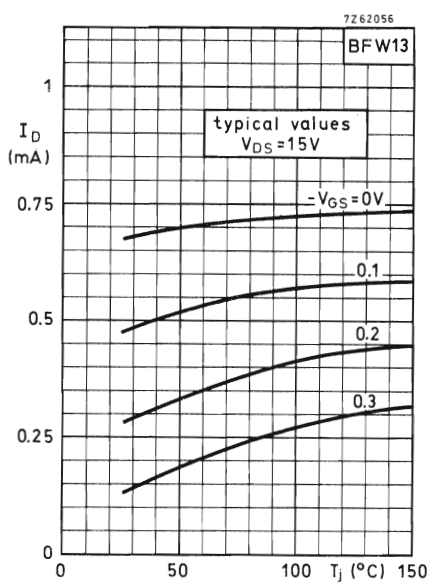
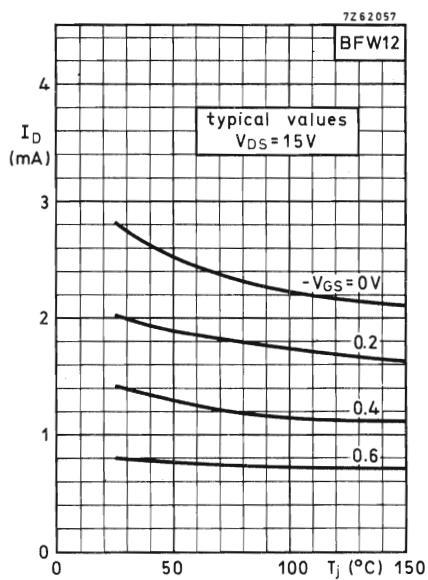
CHARACTERISTICS

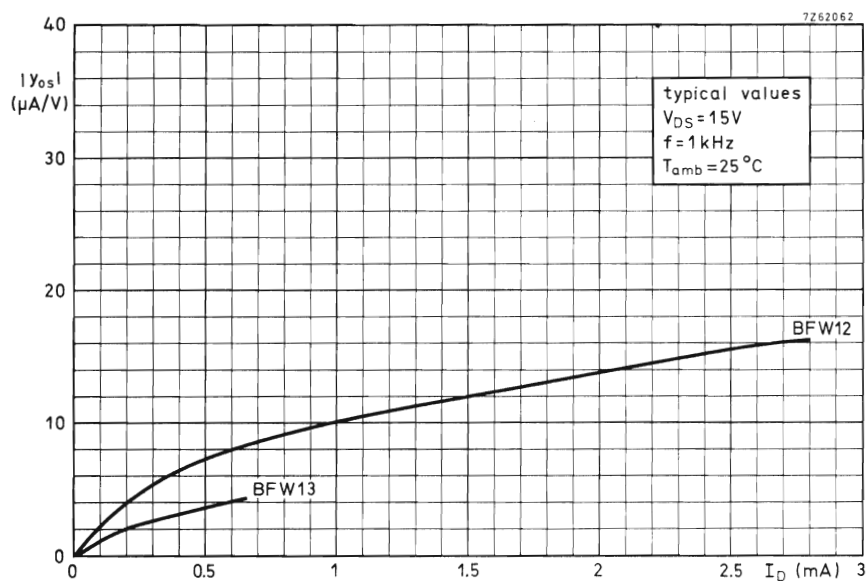
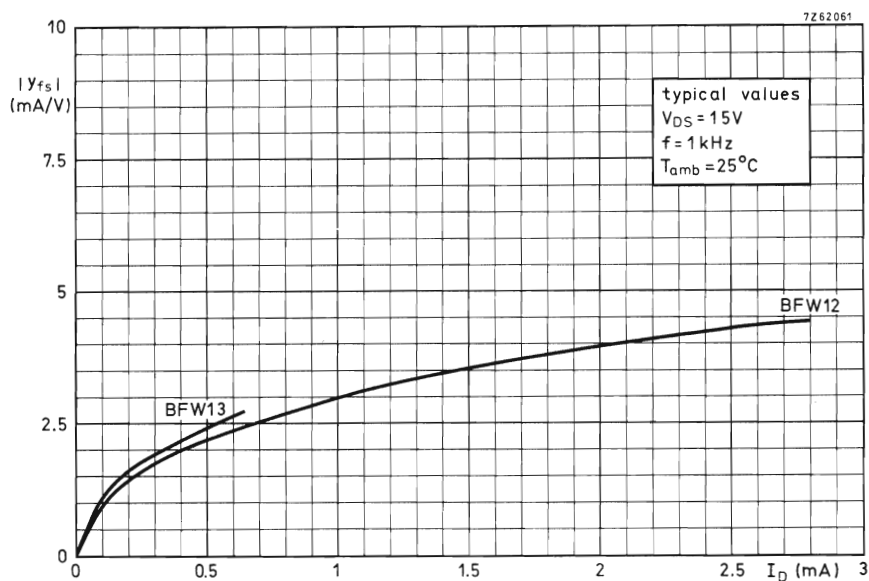
 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

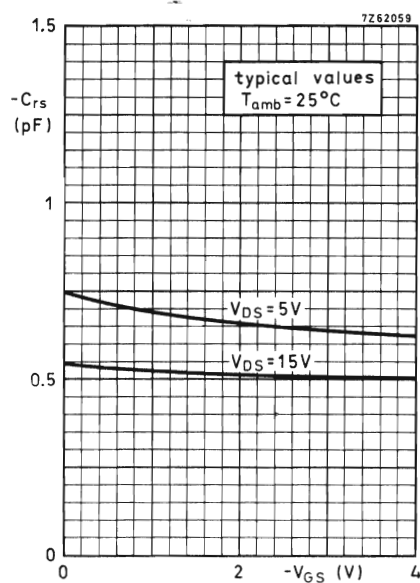
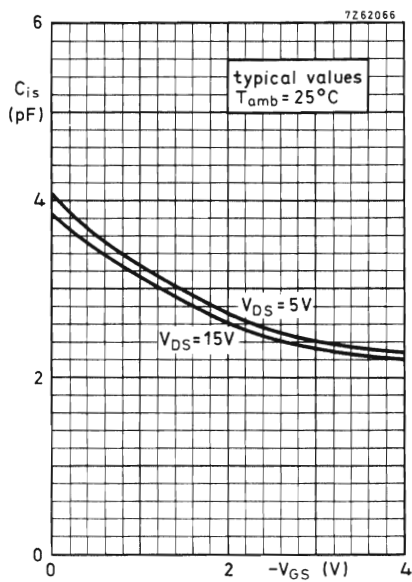
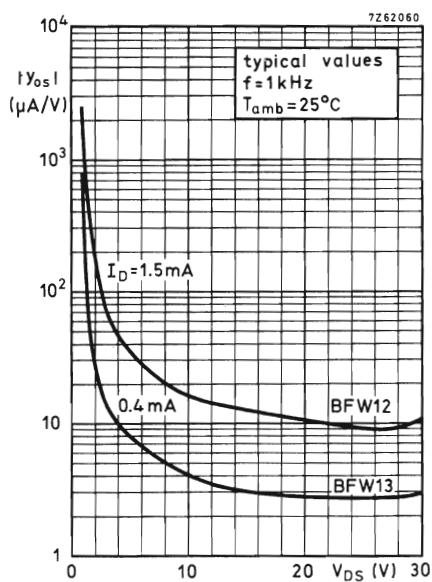
Gate cut-off currents		BFW12		BFW13	
$-V_{GS} = 10\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS} = 10\text{ V}; V_{DS} = 0; T_j = 150\text{ }^{\circ}\text{C}$	$-I_{GSS}$	<	0.1	0.1	μA
Drain current ¹⁾					
$V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}	>	1	0.2	mA
		<	5	1.5	mA
Gate-source voltage					
$I_D = 50\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS}$	>	0.5	0.1	V
		<	2.0	1.0	V
Gate-source cut-off voltage					
$I_D = 0.5\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	<	2.5	1.2	V
y parameters at $f = 1\text{ kHz}; T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$					
$V_{DS} = 15\text{ V}; V_{GS} = 0$					
Transfer admittance	$ y_{fs} $	>	2.0	1.0	mS
Output admittance	$ y_{os} $	<	30	10	μS
$V_{DS} = 15\text{ V}; I_D = 500\text{ }\mu\text{A}$					
Transfer admittance	$ y_{fs} $	>	1.5	–	mS
Output admittance	$ y_{os} $	<	10	–	μS
$V_{DS} = 15\text{ V}; I_D = 200\text{ }\mu\text{A}$					
Transfer admittance	$ y_{fs} $	>	0.5	0.5	mS
Output admittance	$ y_{os} $	<	5	5	μS
$f = 1\text{ MHz}; T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$					
$V_{DS} = 15\text{ V}; V_{GS} = 0$					
Input capacitance	C_{iss}	<	5	5	pF
Feedback capacitance	$-C_{rs}$	<	0.80	0.80	pF
Equivalent noise voltage					
$V_{DS} = 15\text{ V}; I_D = 200\text{ }\mu\text{A}; T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$					
$B = 0.6\text{ to }100\text{ Hz}$	V_n	<	0.5	0.5	μV

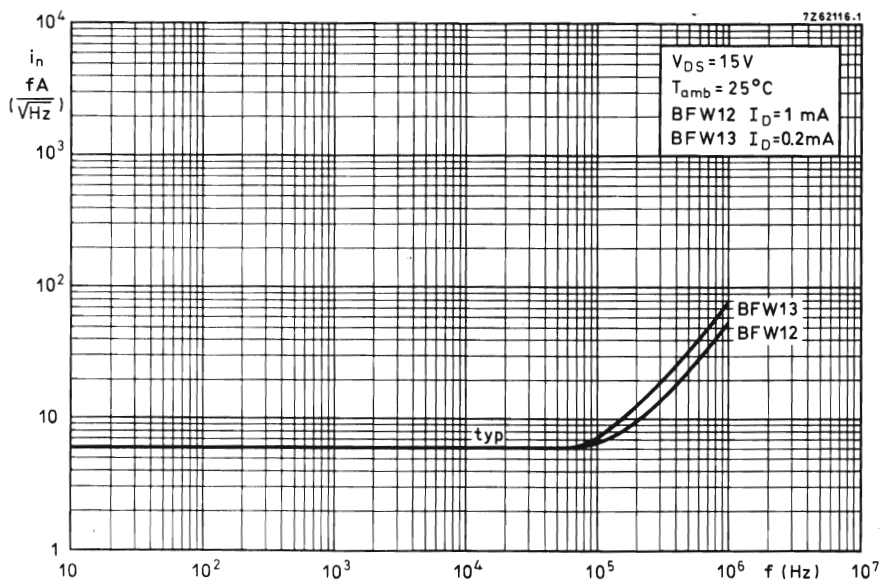
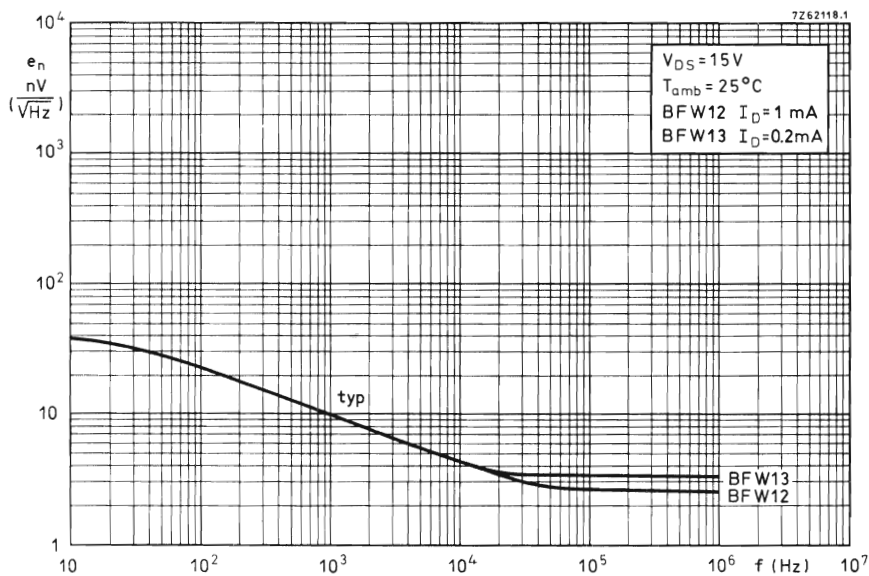
¹⁾ Measured under pulsed conditions.

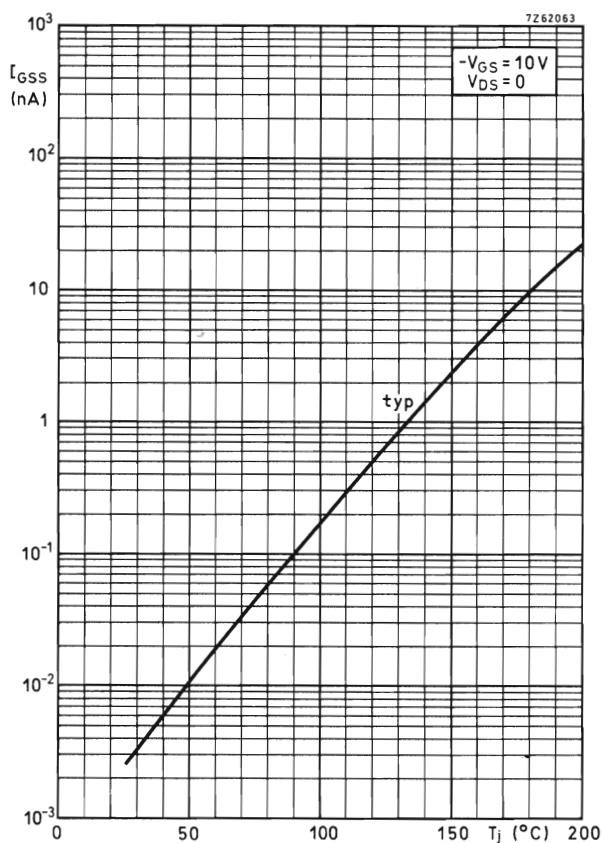












N-CHANNEL SILICON FET

Symmetrical n-channel silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is designed for general purpose amplifiers.

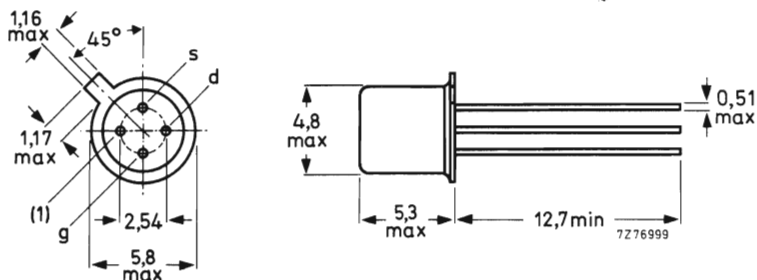
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}		2 to 20 mA
Gate-source cut-off voltage $I_D = 1,0\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	<	8 V
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 15\text{ V}; V_{GS} = 0$	C_{rs}	<	2,0 pF
Transfer admittance (common source) $V_{DS} = 15\text{ V}; V_{GS} = 0; f = 10\text{ MHz}$	$ y_{fs} $	>	1,6 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Drain-gate voltage (open source)	V_{DGO}	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Drain current	I_D	max.	20 mA
Gate current	I_G	max.	10 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
Storage temperature	T_{stg}		-65 to $+200\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	$200\text{ }^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	590 K/W
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CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

 $-V_{GS} = 20\text{ V}; V_{DS} = 0$ $-I_{GSS} < 1,0\text{ nA}$ $-V_{GS} = 20\text{ V}; V_{DS} = 0; T_j = 150\text{ }^{\circ}\text{C}$ $-I_{GSS} < 1,0\text{ }\mu\text{A}$

Drain current*

 $V_{DS} = 15\text{ V}; V_{GS} = 0$ $I_{DSS} \quad 2\text{ to }20\text{ mA}$

Gate-source voltage

 $I_D = 200\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$ $-V_{GS} \quad 0,5\text{ to }7,5\text{ V}$

Gate-source cut-off voltage

 $I_D = 1,0\text{ nA}; V_{DS} = 15\text{ V}$ $-V_{(P)GS} < 8\text{ V}$

y-parameters (common source)

 $V_{DS} = 15\text{ V}; V_{GS} = 0$ Transfer admittance at $f = 1\text{ kHz}$ $|Y_{fs}| \quad 2,0\text{ to }6,5\text{ mS}$ at $f = 10\text{ MHz}$ $> 1,6\text{ mS}$ Output admittance at $f = 1\text{ kHz}$ $|Y_{os}| < 85\text{ }\mu\text{S}$ Input capacitance at $f = 1\text{ MHz}$ $C_{is} < 6\text{ pF}$ Feedback capacitance at $f = 1\text{ MHz}$ $C_{rs} < 2,0\text{ pF}$

* Measured under pulse conditions.

P-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical P-channel junction FETs in a plastic TO-92 envelope and intended for application with analog switches, choppers, commutators etc.

A special feature is the interchangeability of the drain and source connections.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V			
Gate-source voltage	V_{GSO}	max.	30	V			
Gate current	$-I_G$	max.	50	mA			
Total power dissipation up to $T_{amb} = 50\text{ }^{\circ}\text{C}$	P_{tot}	max.	400	mW			
Drain current			BSJ174	BSJ175	BSJ176	BSJ177	
$-V_{DS} = 15\text{ V}; V_{GS} = 0$	$-I_{DSS}$	$>$	20	7	2	1,5	mA
		$<$	135	70	35	20	mA
Drain-source ON-resistance							
$-V_{DS} = 0,1\text{ V}; V_{GS} = 0$	R_{DSon}	$<$	85	125	250	300	Ω

MECHANICAL DATA

Dimensions in mm

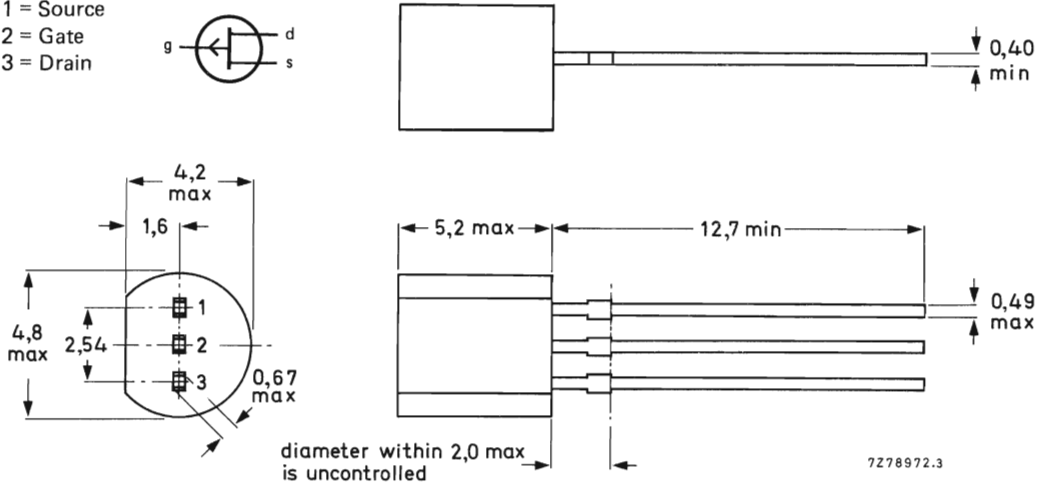
Fig. 1 TO-92.

Pinning:

1 = Source

2 = Gate

3 = Drain



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (d.c.)	$-I_G$	max.	50	mA
Total power dissipation up to $T_{amb} = 50\text{ }^{\circ}\text{C}$	P_{tot}	max.	400	mW
Storage temperature range	T_{stg}		-65 to + 150	$^{\circ}\text{C}$
Junction temperature	T_j	max.	150	$^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	250	K/W
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STATIC CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

		BSJ174 BSJ175 BSJ176 BSJ177			
Gate cut-off current					
$-V_{GS} = 20\text{ V}; V_{DS} = 0$	I_{GSS}	<	1	1	1 nA
Drain cut-off current					
$-V_{DS} = 15\text{ V}; -V_{GS} = 10\text{ V}$	$-I_{DSX}$	<	1	1	1 nA
Drain current					
$-V_{DS} = 15\text{ V}; V_{GS} = 0$	$-I_{DSS}$	>	20	7	2 mA
		<	135	70	35 mA
Gate-source breakdown voltage					
$I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$V_{(BR)GSS}$	>	30	30	30 V
Gate-source cut-off voltage					
$-I_D = 10\text{ nA}; V_{DS} = 0$	$V_{GS\ off}$	>	5	3	0,8 V
		<	10	6	2,25 V
Drain-source ON-resistance					
$-V_{DS} = 0,1\text{ V}; V_{GS} = 0$	R_{DSon}	<	85	125	250 Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz

$-V_{GS} = 10\text{ V}; V_{DS} = 0\text{ V}$

$-V_{GS} = V_{DS} = 0$

C _{is}	typ.	8	pF
C _{is}	typ.	30	pF

Feedback capacitance, f = 1 MHz

$-V_{GS} = 10\text{ V}; V_{DS} = 0\text{ V}$

C _{rs}	typ.	4	pF
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Switching times (see Fig. 2 + 3)

Delay time

t _d	typ.	2	5	15	20	ns
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Rise time

t _r	typ.	5	10	20	25	ns
----------------	------	---	----	----	----	----

Turn-on time

t _{on}	typ.	7	15	35	45	ns
-----------------	------	---	----	----	----	----

Storage time

t _s	typ.	5	10	15	20	ns
----------------	------	---	----	----	----	----

Fall time

t _f	typ.	10	20	20	25	ns
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Turn-off time

t _{off}	typ.	15	30	35	45	ns
------------------	------	----	----	----	----	----

Test conditions:

-V _{DD}	10	6	6	6	V
V _{GSoff}	12	8	6	3	V
R _L	560	1200	2000	2900	Ω
V _{GSon}	0	0	0	0	V

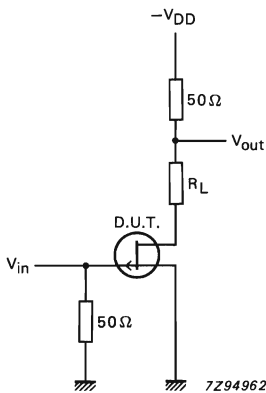


Fig. 2 Switching times test circuit

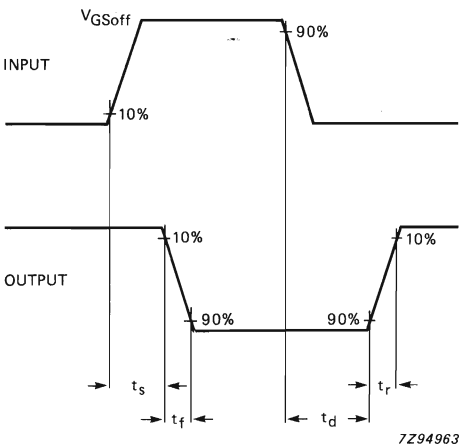


Fig. 3 Input and output waveforms

$t_d + t_r = t_{on}$
 $t_s + t_f = t_{off}$

N-CHANNEL FETS

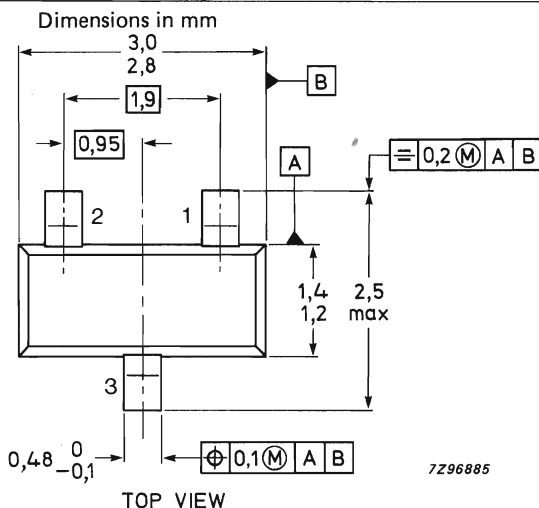
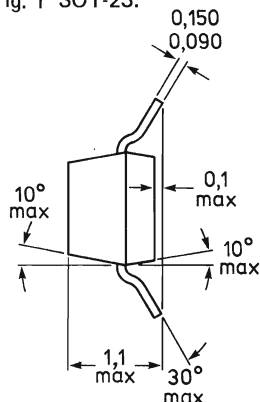
Silicon n-channel depletion type junction field-effect transistors in a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power, chopper or switching applications in industrial service.

QUICK REFERENCE DATA

			BSR56	BSR57	BSR58
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40 V
Total power dissipation up to $T_{amb} = 65^\circ\text{C}$	P_{tot}	max.	250	250	250 mW
Drain current					
$V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}	$>$	50	20	8 mA
		$<$	—	100	80 mA
Gate-source cut-off voltage					
$V_{DS} = 15\text{ V}; I_D = 0,5\text{ nA}$	$-V_{(P)GS}$	$>$	4	2	0,8 V
		$<$	10	6	4 V
Drain-source resistance (on) at $f = 1\text{ kHz}$					
$I_D = 0; V_{GS} = 0$	$r_{ds\text{ on}}$	$<$	25	40	60 Ω
Feedback capacitance at $f = 1\text{ MHz}$					
$-V_{GS} = 10\text{ V}; V_{DS} = 0$	C_{rs}	$<$	5	5	5 pF
Turn-off time					
$V_{DD} = 10\text{ V}; V_{GS} = 0$					
$I_D = 20\text{ mA}; -V_{GSM} = 10\text{ V}$	t_{off}	$<$	25	—	— ns
$I_D = 10\text{ mA}; -V_{GSM} = 6\text{ V}$	t_{off}	$<$	—	50	— ns
$I_D = 5\text{ mA}; -V_{GSM} = 4\text{ V}$	t_{off}	$<$	—	—	100 ns

MECHANICAL DATA

Fig. 1 SOT-23.



Marking code

BSR56 = M4
BSR57 = M5
BSR58 = M6



7Z96885

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage (See Fig. 4)	$\pm V_{DS}$	max.	40 V
Drain-gate voltage (See Fig. 4)	V_{DGO}	max.	40 V
Gate-source voltage (See Fig. 4)	$-V_{GSO}$	max.	40 V
Forward gate current	I_{GF}	max.	50 mA
Total power dissipation up to $T_{amb} = 65^\circ\text{C}$	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}	—55 to + 175	$^\circ\text{C}$
Junction temperature	T_j	max.	175 $^\circ\text{C}$

THERMAL CHARACTERISTICS*

$$T_j = P (R_{th j-t} + R_{th t-s} + R_{th s-a}) + T_{amb}$$

Thermal resistance

From junction to tab	$R_{th j-t}$	=	60 K/W
From tab to soldering points	$R_{th t-s}$	=	280 K/W
From soldering points to ambient**	$R_{th s-a}$	=	90 K/W

CHARACTERISTICS

$T_{amb} = 25^\circ\text{C}$ unless otherwise specified

Gate-source cut-off current $V_{DS} = 0\text{ V}; -V_{GS} = 20\text{ V}$	$-I_{GSS}$	<	1	nA
Drain cut-off current $V_{DS} = 15\text{ V}; -V_{GS} = 10\text{ V}$	I_{DSX}	<	1	nA

			BSR56	BSR57	BSR58
Drain current Δ $V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}	$>$ $<$	50 —	20 100	8 mA 80 mA
Gate-source breakdown voltage $-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	$>$	40	40	40 V
Gate-source cut-off voltage $I_D = 0,5\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	$>$ $<$	4 10	2 6	0,8 V 4 V
Drain-source voltage (on) $I_D = 20\text{ mA}; V_{GS} = 0$	V_{DSon}	$<$	750	—	— mV
$I_D = 10\text{ mA}; V_{GS} = 0$	V_{DSon}	$<$	—	500	— mV
$I_D = 5\text{ mA}; V_{GS} = 0$	V_{DSon}	$<$	—	—	400 mV
Drain-source resistance (on) at $f = 1\text{ kHz}$ $I_D = 0; V_{GS} = 0$	$r_{ds on}$	$<$	25	40	60 Ω

* See *Thermal characteristics*.

** Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Δ Measured under pulsed conditions; $t_p = 100\text{ ms}; \delta \leq 0,1$.

Switching times*

 $V_{DD} = 10\text{ V}; V_{GS} = 0$ Conditions I_D and $-V_{GSM}$

Delay time

Rise time

Turn-off time

 I_D
 $-V_{GSM}$

=

=

<

<

<

BSR56

BSR57

BSR58

20

10

5 mA

10

6

4 V

6

6

10 ns

3

4

10 ns

25

50

100 ns

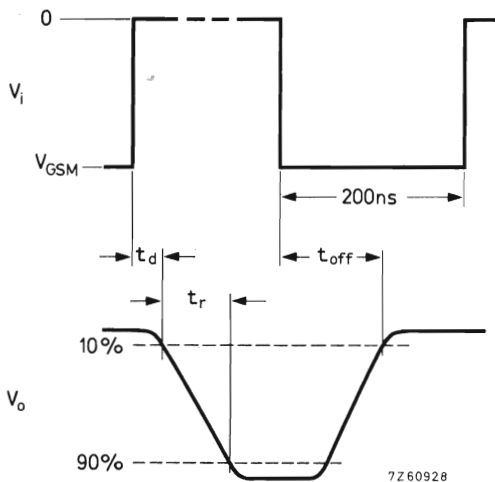


Fig. 2 Switching times waveforms.

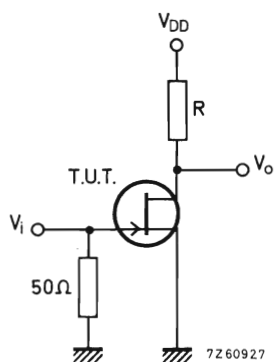


Fig. 3 Test circuit.

BSR56; $R = 464\ \Omega$
 BSR57; $R = 953\ \Omega$
 BSR58; $R = 1910\ \Omega$

Pulse generator

 $t_r = t_f \leq 1\text{ ns}$ $\delta = 0,02$ $Z_o = 50\ \Omega$

Oscilloscope

 $t_r \leq 0,75\text{ ns}$ $R_i \geq 1\text{ M}\Omega$ $C_i \leq 2,5\text{ pF}$

* Switching times measured on devices in SOT-18 envelope.

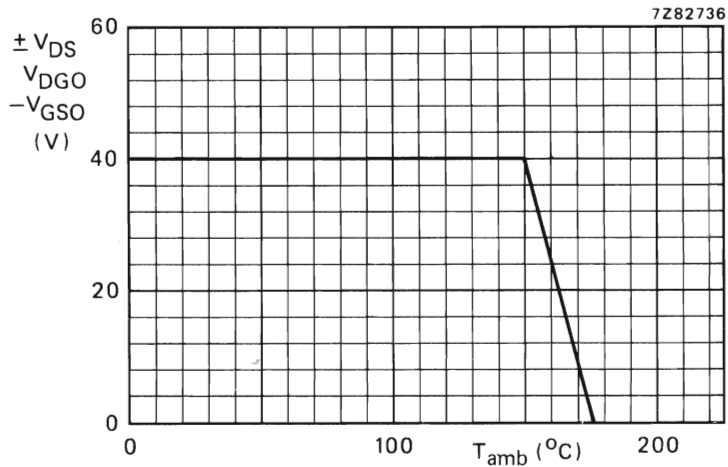


Fig. 4 Voltage derating curve.

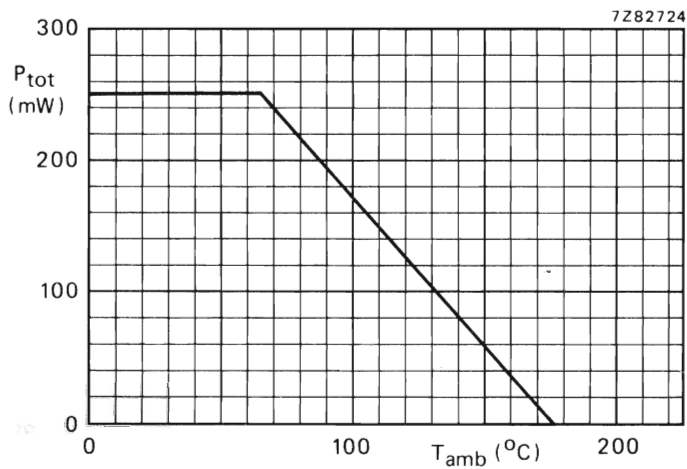


Fig. 5 Power derating curve.

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

BSR174 to 177

P-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical p-channel junction FETs in plastic microminiature SOT-23 envelopes and containing a BSR174, 175, 176 or 177 crystal.

They are intended for application with analogue switches, choppers, commutators etc. using SMD technology.

A special feature is the interchangeability of the drain and source connections.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GS0}	max.	30	V
Gate current	$-I_G$	max.	50	mA
Total power dissipation up to $T_{amb} = 25^\circ\text{C}$	P_{tot}	max.	300	mW

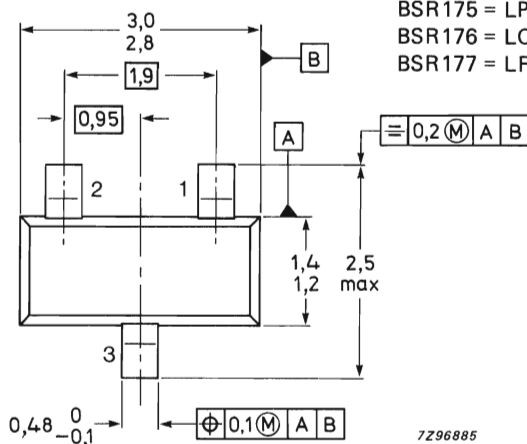
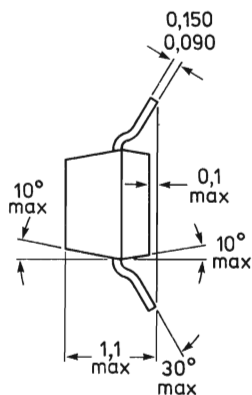
		BSR174	BSR175	BSR176	BSR177	
Drain current						
$-V_{DS} = 15\text{ V}; V_{GS} = 0$	$-I_{DSS}$	> 20	7	2	1,5	mA
		< 135	70	35	20	mA
Drain-source ON-resistance						
$-V_{DS} = 0,1\text{ V}; V_{GS} = 0$	$R_{DS\text{ on}}$	< 85	125	250	300	Ω

MECHANICAL DATA

Fig. 1 SOT-23.

Pinning:

- 1 = Drain
- 2 = Source
- 3 = Gate



Dimensions in mm

Marking codes:

BSR174 = LO

BSR175 = LP

BSR176 = LQ

BSR177 = LR

TOP VIEW

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GS0}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (d.c.)	$-I_G$	max.	50	mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$ *	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		-65 to + 150	$^{\circ}\text{C}$
Junction temperature	T_j	max.	150	$^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air	R_{thj-a}	=	430	K/W
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STATIC CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

			BSR174	BSR175	BSR176	BSR177
Gate cut-off current $-V_{GS} = 20\text{ V}; V_{DS} = 0$	I_{GSS}	<	1	1	1	1 nA
Drain cut-off current $-V_{DS} = 15\text{ V}; -V_{GS} = 10\text{ V}$	$-I_{DSX}$	<	1	1	1	1 nA
Drain current $-V_{DS} = 15\text{ V}; V_{GS} = 0$	$-I_{DSS}$	> <	20 135	7 70	2 35	1,5 20 mA
Gate-source breakdown voltage $I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$V_{(BR)GSS}$	>	30	30	30	30 V
Gate-source cut-off voltage $-I_D = 10\text{ nA}; V_{DS} = 0$	$V_{GS\text{ off}}$	> <	5 10	3 6	1 4	0,8 2,25 V
Drain-source ON-resistance $-V_{DS} = 0,1\text{ V}; V_{GS} = 0$	$R_{DS\text{ on}}$	<	85	125	250	300 Ω

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

DYNAMIC CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

Input capacitance, $f = 1\text{ MHz}$

$-V_{GS} = 10\text{ V}; V_{DS} = 0\text{ V}$

$-V_{GS} = V_{DS} = 0$

Feedback capacitance, $f = 1\text{ MHz}$

$-V_{GS} = 10\text{ V}; V_{DS} = 0\text{ V}$

Switching times (see Fig. 2 + 3)

Delay time

Rise time

Turn-on time

Storage temperature

Fall time

Turn-off time

Test conditions:

		BSR174	BSR175	BSR176	BSR177
C_{is}	typ.	2	5	15	20
C_{is}	typ.	5	10	20	25
C_{rs}	typ.	7	15	35	45
t_d	typ.	5	10	15	20
t_r	typ.	10	20	20	25
t_{on}	typ.	15	30	35	45
t_s	typ.	5	10	15	20
t_f	typ.	10	20	20	25
t_{off}	typ.	15	30	35	45
$-V_{DD}$		10	6	6	6
$V_{GS\text{ off}}$		12	8	6	3
R_L		560	1200	2000	2900
$V_{GS\text{ on}}$		0	0	0	0

DEVELOPMENT DATA

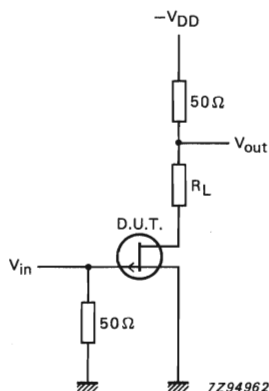


Fig. 2 Switching times test circuit

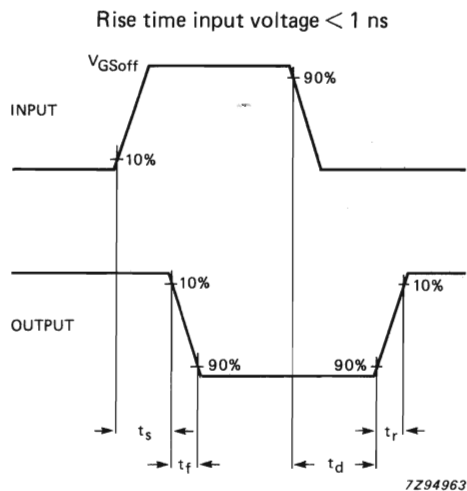


Fig. 3 Input and output waveforms

$$t_d + t_r = t_{on}$$

$$t_s + t_f = t_{off}$$

N-CHANNEL FETS



Silicon symmetrical n-channel junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for switching applications. The devices have the feature: low 'on' resistance at zero gate voltage.

QUICK REFERENCE DATA

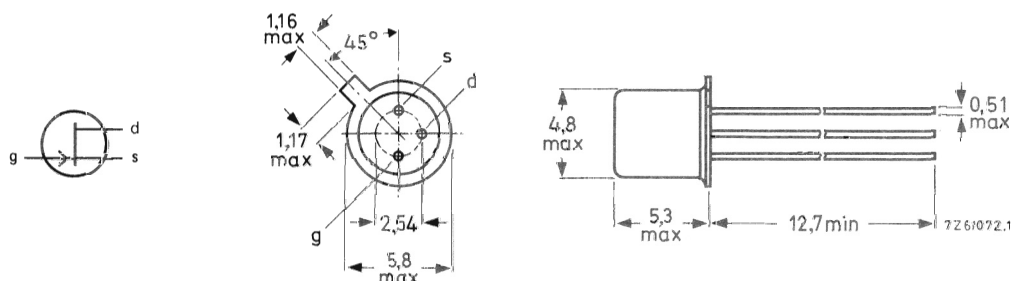
Drain-source voltage	$\pm V_{DS}$	max.	40	V		
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	350	mW		
Drain current			BSV78	BSV79	BSV80	
$V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage						
$I_D = 1\text{ nA}; V_{GS} = 15\text{ V}$	$-V_{(P)GS}$	>	3,75	2,0	1,0	V
		<	11	7,0	5,0	V
Drain-source resistance (on) at $f = 1\text{ kHz}$						
$I_D = 0; V_{GS} = 0$	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at $f = 1\text{ MHz}$						
$V_{DS} = 0; -V_{GS} = 10\text{ V}$	C_{rs}	<	5	5	5	pF
Turn-on time	t_{on}	<	10	18	30	ns
Turn-off time	t_{off}	<	10	16	32	ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case



Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).



Products approved to CECC 50 012-011, available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40 V
Drain-gate voltage (open source)	V_{DGO}	max.	40 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40 V
Forward gate current	I_G	max.	50 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	350 mW
Storage temperature	T_{stg}	$-65\text{ to }+200\text{ }^{\circ}\text{C}$	
Operating junction temperature	T_j	max.	175 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	430 K/W
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CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	0.25	nA
$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_j = 150\text{ }^{\circ}\text{C}$	$-I_{GSS}$	<	0.5	μA

Drain cut-off current

$V_{DS} = 15\text{ V}; -V_{GS} = 12\text{ V}$	I_{DSX}	<	0.25	nA
$V_{DS} = 15\text{ V}; -V_{GS} = 12\text{ V}; T_j = 150\text{ }^{\circ}\text{C}$	I_{DSX}	<	0.5	μA

Drain current

			BSV78	BSV79	BSV80
$V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}	>	50	20	10 mA

Gate-source cut-off voltage

$I_D = 1\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS}$	>	3.75	2.0	1.0 V
		<	11	7.0	5.0 V

Gate-source voltage

$I_D = 1.5\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS}$	>	3.5	1.75	0.75 V
		<	10	6.0	4.0 V

Drain-source voltage (on)

$I_D = 20\text{ mA}; V_{GS} = 0$	V_{DSon}	<	500		mV
$I_D = 10\text{ mA}; V_{GS} = 0$	V_{DSon}	<		400	mV
$I_D = 5\text{ mA}; V_{GS} = 0$	V_{DSon}	<			325 mV

Drain-source resistance (on) at $f = 1\text{ kHz}$

$I_D = 0; V_{GS} = 0$	$r_{ds\text{ on}}$	<	25	40	60 Ω
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y parameters at $f = 1\text{ MHz}$ (common source)

$-V_{GS} = 10\text{ V}; V_{DS} = 0$					
Input capacitance	C_{is}	<	10	10	10 pF
Feedback capacitance	$-C_{rs}$	<	5	5	5 pF

Switching times (see Fig. 2)

Turn-on time when switched from

- V_{GSMoff} = 11 V to I_{Don} = 20 mA; V_{DD} = 10 V (BSV78)
- V_{GSMoff} = 7 V to I_{Don} = 10 mA; V_{DD} = 10 V (BSV79)
- V_{GSMoff} = 5 V to I_{Don} = 5 mA; V_{DD} = 10 V (BSV80)

- delay time
- rise time
- turn-on time

Turn-off time when switched from

- I_{Don} = 20 mA to -V_{GSMoff} = 11 V; V_{DD} = 10 V (BSV78)
- I_{Don} = 10 mA to -V_{GSMoff} = 7 V; V_{DD} = 10 V (BSV79)
- I_{Don} = 5 mA to -V_{GSMoff} = 5 V; V_{DD} = 10 V (BSV80)

- fall time
- storage time
- turn-off time

	BSV78	BSV79	BSV80
t _d	< 5	10	10 ns
t _r	< 5	8	20 ns
t _{on}	< 10	18	30 ns
t _f	< 6	11	24 ns
t _s	< 4	5	8 ns
t _{off}	< 10	16	32 ns

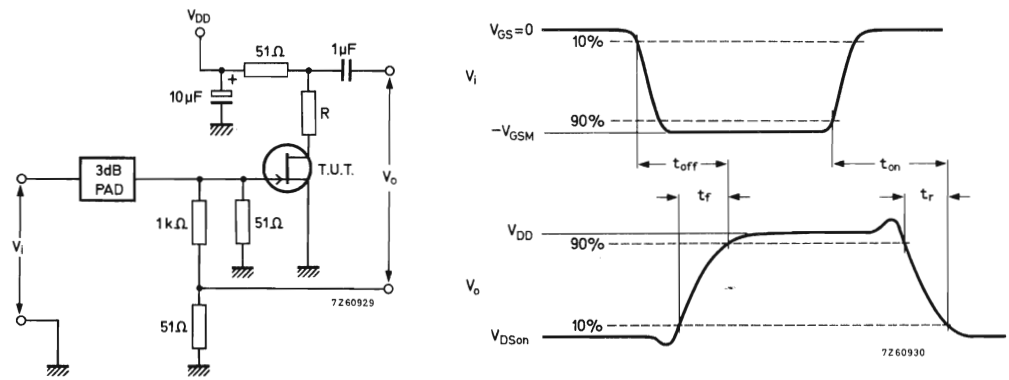


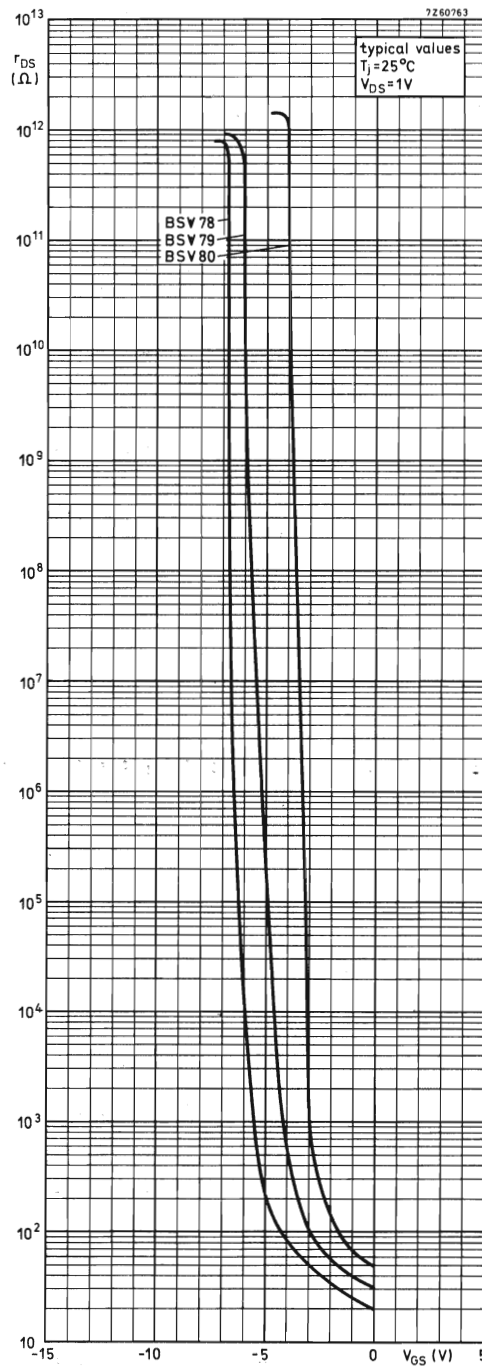
Fig. 2 Switching times test circuit and input and output waveforms.

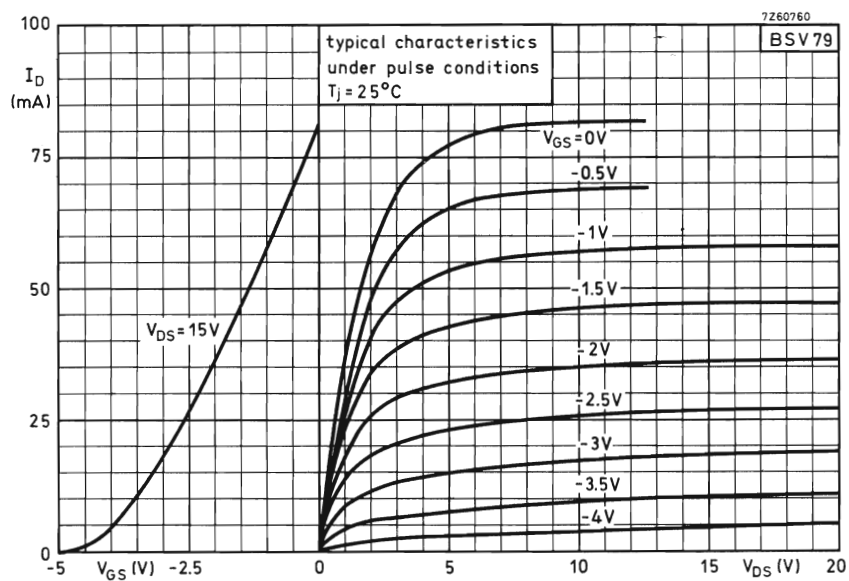
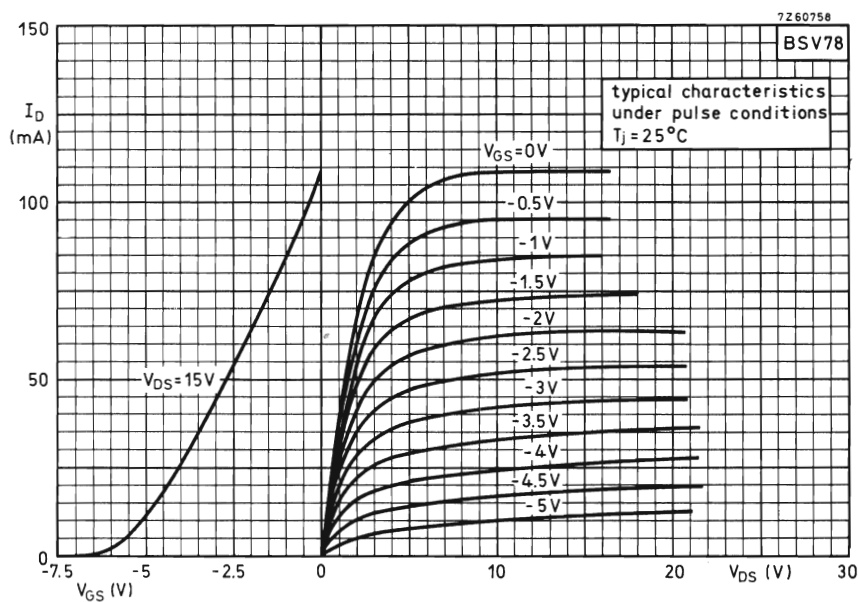
$$R = \frac{10 - V_{DSon} (V)}{I_{Don} (A)} - 51$$

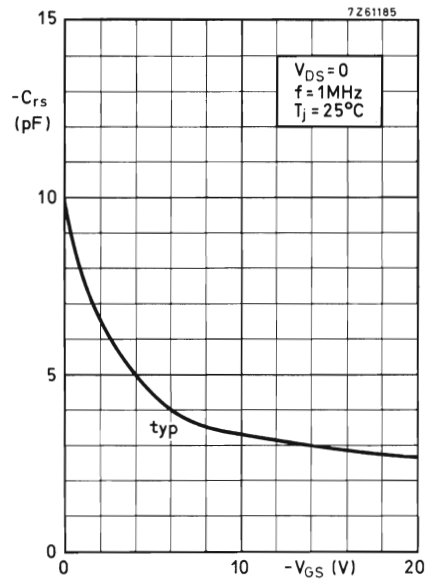
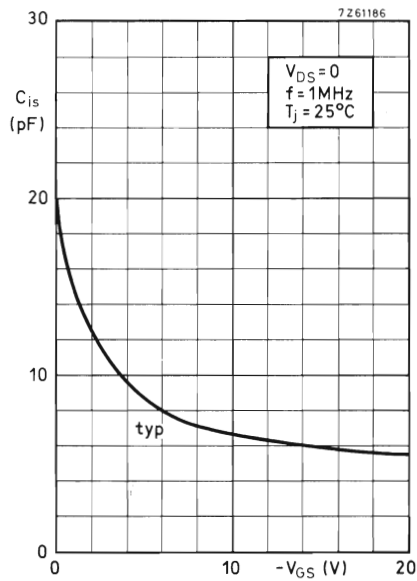
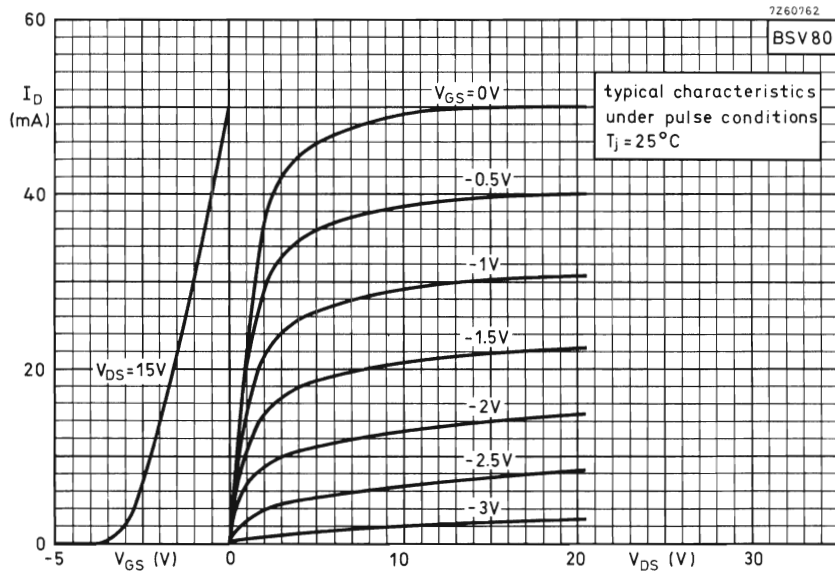
	BSV78	BSV79	BSV80
R	= 424	909	1885 Ω

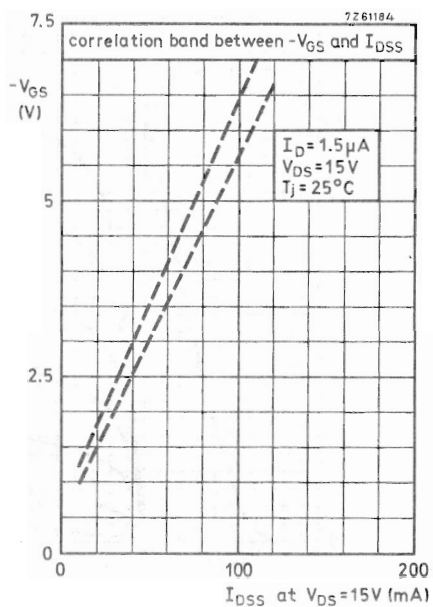
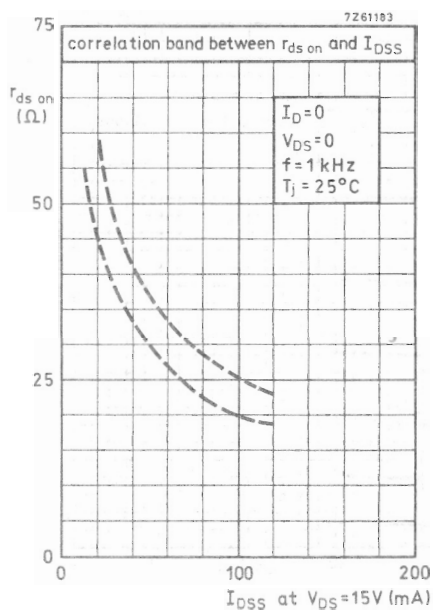
Pulse generator:
R_i = 50 Ω
t_r < 0,5 ns
t_f < 5 ns

Oscilloscope:
R_i = 50 Ω
t_r < 1 ns
t_f < 1 ns









N-CHANNEL FETS

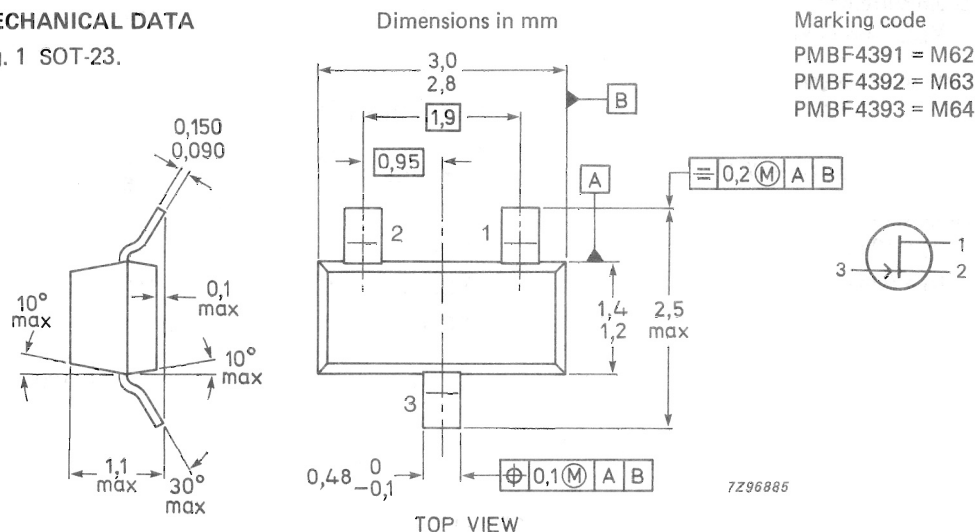
Symmetrical silicon n-channel depletion type junction field-effect transistors on a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power chopper or switching applications in industry.

QUICK REFERENCE DATA

			PMBF4391	PMBF4392	PMBF4393
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40 V
Drain current					
$V_{DS} = 20 \text{ V}; V_{GS} = 0$	I_{DSS}	$>$	50	25	5 mA
Gate-source cut-off voltage					
$V_{DS} = 20 \text{ V}; I_D = 1 \text{ nA}$	$-V_{(P)GS}$	$>$	4	2	0,5 V
		$<$	10	5	3 V
Drain-source resistance (on) at $f = 1 \text{ kHz}$					
$I_D = 1 \text{ mA}; V_{GS} = 0$	$r_{ds\ on}$	$<$	30	60	100 Ω
Feedback capacitance at $f = 1 \text{ MHz}$					
$-V_{GS} = 12 \text{ V}; V_{DS} = 0$	C_{rs}	$<$	3,5	3,5	3,5 pF
Turn-off time					
$V_{DD} = 10 \text{ V}; V_{GS} = 0$					
$I_D = 12 \text{ mA}; -V_{GSM} = 12 \text{ V}$	t_{off}	$<$	20	—	— ns
$I_D = 6 \text{ mA}; -V_{GSM} = 7 \text{ V}$	t_{off}	$<$	—	35	— ns
$I_D = 3 \text{ mA}; -V_{GSM} = 5 \text{ V}$	t_{off}	$<$	—	—	50 ns

MECHANICAL DATA

Fig. 1 SOT-23.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage (See Fig. 4)	$\pm V_{DS}$	max.	40 V
Drain-gate voltage (See Fig. 4)	V_{DGO}	max.	40 V
Gate-source voltage (See Fig. 4)	$-V_{GSO}$	max.	40 V
Gate current (d.c.)	I_G	max.	50 mA
Total power dissipation up to $T_{amb} = 65^\circ\text{C}$	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		-65 to $+175^\circ\text{C}$
Junction temperature	T_j	max.	175°C

THERMAL CHARACTERISTICS

$$T_j = P (R_{th j-t} + R_{th t-s} + R_{th s-a}) + T_{amb}$$

Thermal resistance

From junction to tab	$R_{th j-t}$	=	60 K/W
From tab to soldering points	$R_{th t-s}$	=	260 K/W
From soldering points to ambient *	$R_{th s-a}$	=	120 K/W

CHARACTERISTICS

$T_{amb} = 25^\circ\text{C}$ unless otherwise specified

Gate-source voltage

$$I_G = 1 \text{ mA}; V_{DS} = 0$$

$$V_{Gson} < 1 \text{ V}$$

Gate-source cut-off current

$$V_{DS} = 0 \text{ V}; -V_{GS} = 20 \text{ V}$$

$$-I_{GSS} < 1 \text{ nA}$$

$$V_{DS} = 0 \text{ V}; -V_{GS} = 20 \text{ V}; T_{amb} = 150^\circ\text{C}$$

$$-I_{GSS} < 0,2 \mu\text{A}$$

		PMBF4391	PMBF4392	PMBF4393
Drain current**	I_{DSS}	> 50	25	5 mA
		< 150	75	30 mA
Gate-source breakdown voltage	$-V_{(BR)GSS}$	> 40	40	40 V
$-I_G = 1 \mu\text{A}; V_{DS} = 0$				
Gate-source cut-off voltage	$-V_{(P)GS}$	> 4	2	0,5 V
		< 10	5	3 V
Drain-source voltage (on)	V_{DSon}	$< 0,4$	—	— V
	V_{DSon}	$< 0,4$	0,4	— V
	V_{DSon}	$< 0,4$	—	0,4 V
Drain-source resistance (on)	$r_{ds on}$	< 30	60	100 Ω

* Mounted on a ceramic substrate of 7 mm x 5 mm x 0,7 mm.

** Measured under pulsed conditions; $t_p = 100 \mu\text{s}$; $\delta = 0,01$.

		PMBF4391	PMBF4392	PMBF4393	
Drain cut-off current					
$-V_{GS} = 12\text{ V}$	$V_{DS} = 20\text{ V}$	I_{DSX}	< 1	—	— nA
$-V_{GS} = 7\text{ V}$		I_{DSX}	< —	1	— nA
$-V_{GS} = 5\text{ V}$		I_{DSX}	< —	—	1 nA
$-V_{GS} = 12\text{ V}$	$V_{DS} = 20\text{ V}; T_{amb} = 150^{\circ}\text{C}$	I_{DSX}	< 0,2	—	— μA
$-V_{GS} = 7\text{ V}$		I_{DSX}	< —	0,2	— μA
$-V_{GS} = 5\text{ V}$		I_{DSX}	< —	—	0,2 μA
y-parameters (common source)					
$V_{DS} = 20\text{ V}; V_{GS} = 0; f = 1\text{ MHz}$					
Input capacitance	C_{is}	< 14	14	14	pF
Feedback capacitance	C_{rs}	< 3,5	3,5	3,5	pF
Switching times					
$V_{DD} = 10\text{ V}; V_{GS} = 0$					
Conditions I_D and $-V_{GSM}$	I_D	= 12	6	3	mA
	$-V_{GSM}$	= 12	7	5	V
Rise time	t_r	< 5	5	5	ns
Turn on time	t_{on}	< 15	15	15	ns
Fall time	t_f	< 15	20	30	ns
Turn off time	t_{off}	< 20	35	50	ns

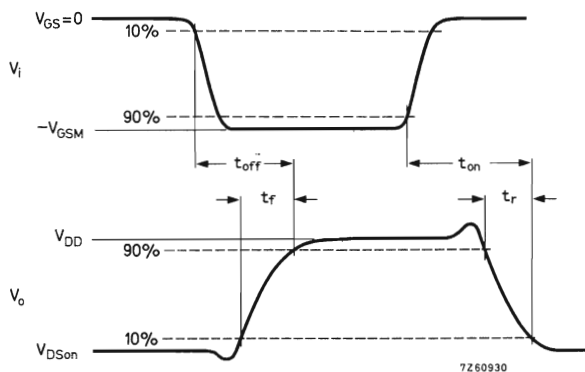
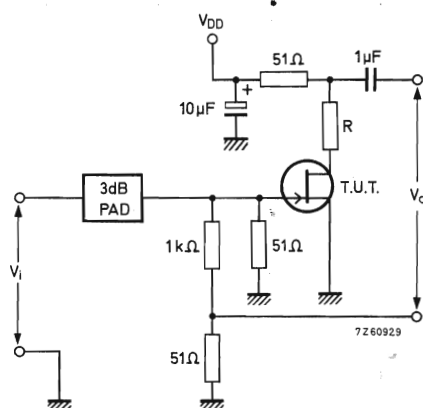


Fig. 2 Switching times waveforms.



$$R = \frac{9,6}{I_D} - 51 \Omega$$

Pulse generator:

$$\begin{aligned} t_r &< 0,5 \text{ ns} \\ t_f &< 0,5 \text{ ns} \\ t_p &= 100 \mu\text{s} \\ \delta &= 0,01 \end{aligned}$$

Oscilloscope:

$$R_i = 50 \Omega$$

Fig. 3 Test circuit.

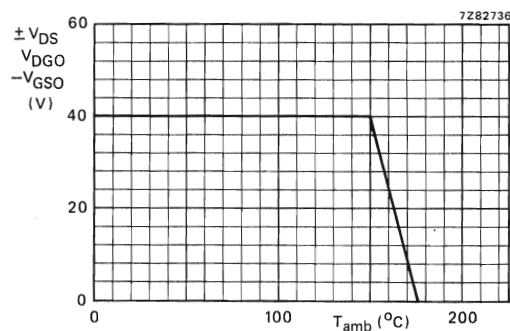


Fig. 4 Voltage derating curve.

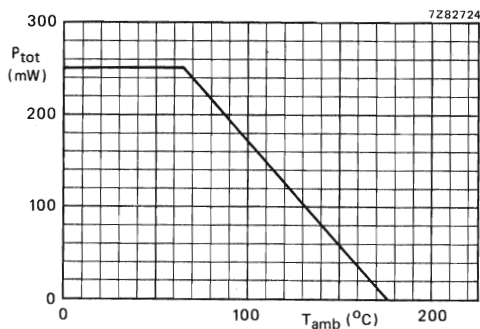


Fig. 5 Power derating curve.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon junction field-effect transistor, designed primarily for small-signal general purpose high-frequency amplifier applications. The 2N3822 features low gate leakage current and low input capacitance.

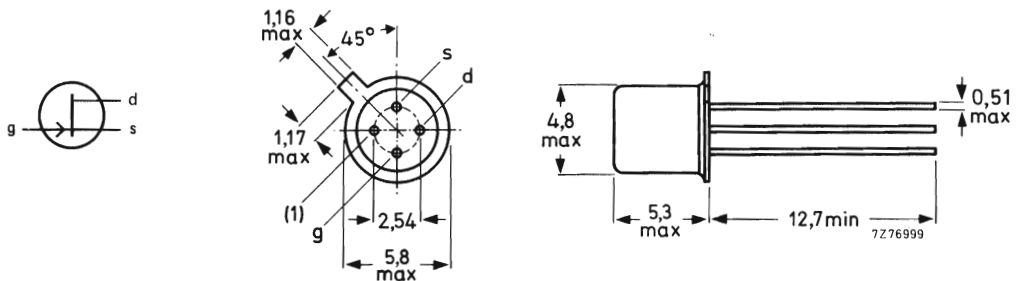
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	50 V
Gate-source voltage	$-V_{GS}$	max.	50 V
Total power dissipation up to $T_{amb} = 25^\circ\text{C}$	P_{tot}	max.	300 mW
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}		2 to 10 mA
Transfer admittance (common source) $V_{DS} = 15\text{ V}; V_{GS} = 0; f = 1\text{ kHz}$	$ y_{fs} $		3,0 to 6,5 mS
$V_{DS} = 15\text{ V}; V_{GS} = 0; f = 100\text{ MHz}$	$ y_{fs} $	>	3,0 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



Note: Drain and source are interchangeable.

(1) Shield lead connected to case.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	50 V
Drain-gate voltage	V_{DG}	max.	50 V
Gate-source voltage	$-V_{GS}$	max.	50 V
Gate current (d.c.)	I_G	max.	10 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
Storage temperature	T_{stg}		-65 to $+200\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	$200\text{ }^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	590 K/W
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CHARACTERISTICS with source connected to case for all measurements $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off current

$-V_{GS} = 30\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	0,1 nA
$-V_{GS} = 30\text{ V}; V_{DS} = 0; T_{amb} = 150\text{ }^{\circ}\text{C}$	$-I_{GSS}$	<	0,1 μA

Drain current *

$V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}		2 to 10 mA
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Gate-source breakdown voltage

$-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	>	50 V
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Gate-source voltage

$V_{DS} = 15\text{ V}; I_D = 200\text{ }\mu\text{A}$	$-V_{GS}$		1 to 4 V
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Gate-source cut-off voltage

$V_{DS} = 15\text{ V}; I_D = 0,5\text{ nA}$	$-V_{(P)GS}$	<	6 V
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Small-signal common source characteristics $V_{DS} = 15\text{ V}; V_{GS} = 0$

Transfer admittance *

$f = 1\text{ kHz}$	$ Y_{fs} $		3,0 to 6,5 mS
$f = 100\text{ MHz}$	$ Y_{fs} $	>	3,0 mS

Output admittance at $f = 1\text{ kHz}$ *

$ Y_{os} $	<	20 μS
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Input capacitance at $f = 1\text{ MHz}$

C_{is}	<	6 pF
----------	---	------

Feedback capacitance at $f = 1\text{ MHz}$

C_{rs}	<	3 pF
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Noise figure

$V_{DS} = 15\text{ V}; V_{GS} = 0; R_G = 1\text{ M}\Omega$			
$f = 10\text{ Hz}; B = 5\text{ Hz}$	F	<	5 dB

Equivalent input noise voltage

$V_{DS} = 15\text{ V}; V_{GS} = 0$			
$f = 10\text{ Hz}; B = 5\text{ Hz}$	V_n	<	$200\text{ nV}/\sqrt{\text{Hz}}$

* Measured under pulse conditions: $t_p = 100\text{ ms}; \delta \leq 0,1$.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope, intended for v.h.f. amplifier and mixer applications in industrial service.

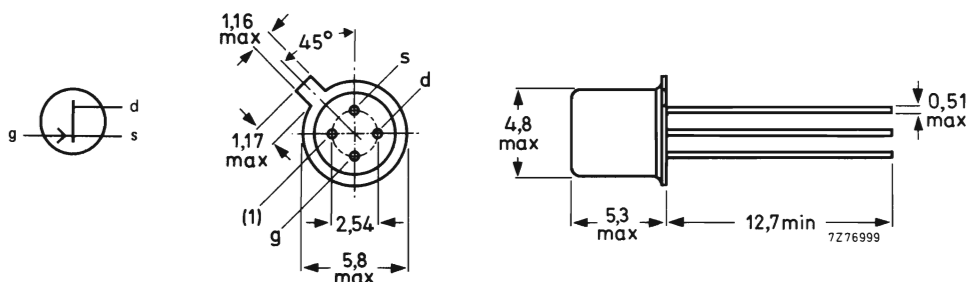
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Gate-source voltage	$-V_{GS}$	max.	30 V
Total power dissipation up to $T_{amb} = 25^{\circ}\text{C}$	P_{tot}	max.	300 mW
Drain current $V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}		4 to 20 mA
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 15\text{ V}; V_{GS} = 0$	C_{rs}	<	2 pF
Transfer admittance (common source) $V_{DS} = 15\text{ V}; V_{GS} = 0; f = 200\text{ MHz}$	$ y_{fs} $	>	3,2 mS
Noise figure at $f = 100\text{ MHz}$ $V_{DS} = 15\text{ V}; V_{GS} = 0; R_G = 1\text{ k}\Omega$	F	<	2,5 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



Note: Drain and source are interchangeable.

(1) Shield lead connected to case.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage	V_{DG}	max.	30 V
Gate-source voltage	$-V_{GS}$	max.	30 V
Gate current (d.c.)	I_G	max.	10 mA
Total power dissipation up to $T_{amb} = 25^\circ\text{C}$	P_{tot}	max.	300 mW
Storage temperature	T_{stg}		-65 to $+200^\circ\text{C}$
Junction temperature	T_j	max.	200°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	590 K/W
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CHARACTERISTICS with source and shield connected to case for all measurements

 $T_{amb} = 25^\circ\text{C}$ unless otherwise specified

Gate cut-off current

$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	0,5 nA
$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_{amb} = 150^\circ\text{C}$	$-I_{GSS}$	<	0,5 μA

Drain current *

$V_{DS} = 15\text{ V}; V_{GS} = 0$	I_{DSS}		4 to 20 mA
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Gate-source breakdown voltage

$-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	>	30 V
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Gate-source voltage

$I_D = 400\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$	$-V_{GS}$		1,0 to 7,5 V
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Gate-source cut-off voltage

$V_{DS} = 15\text{ V}; I_D = 0,5\text{ nA}$	$-V_{(P)GS}$	<	8 V
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Small-signal common source characteristics

 $V_{DS} = 15\text{ V}; V_{GS} = 0$

Transfer admittance *

$f = 1\text{ kHz}$	$ Y_{fs} $		3,5 to 6,5 mS
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$f = 200\text{ MHz}$	$ Y_{fs} $	>	3,2 mS
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Output admittance at $f = 1\text{ kHz}$ *

$ Y_{os} $	<	35 μS
------------	---	------------------

Input capacitance at $f = 1\text{ MHz}$

C_{is}	<	6 pF
----------	---	------

Feedback capacitance at $f = 1\text{ MHz}$

C_{rs}	<	2 pF
----------	---	------

Real part of input conductance at $f = 200\text{ MHz}$

$\text{Re}(Y_{is})$	<	0,8 mS
---------------------	---	--------

Real part of output conductance at $f = 200\text{ MHz}$

$\text{Re}(Y_{os})$	<	0,2 mS
---------------------	---	--------

Noise figure at $f = 100\text{ MHz}$

$V_{DS} = 15\text{ V}; V_{GS} = 0; R_G = 1\text{ k}\Omega$	F	<	2,5 dB
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* Measured under pulse conditions: $t_p = 100\text{ ms}; \delta \leq 0,1$.

N-CHANNEL SILICON FET

Symmetrical n-channel planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is suitable in a variety of low power switching applications, e.g. in multiplexing systems.

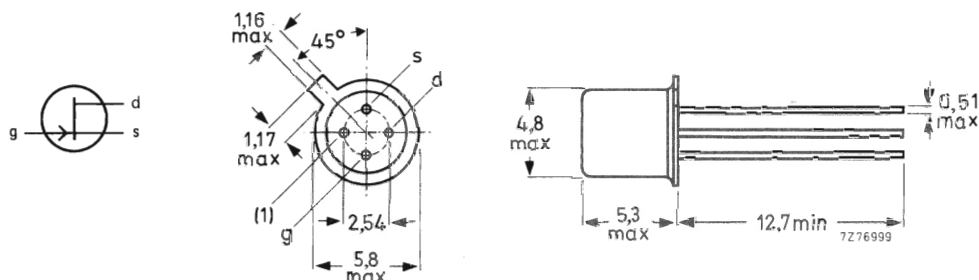
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Total power dissipation up to $T_{amb} = 25^{\circ}\text{C}$	P_{tot}	max.	300 mW
Drain current $V_{DS} = 20\text{ V}; V_{GS} = 0$	I_{DSS}	>	2 mA
Gate-source cut-off voltage $I_D = 10\text{ nA}; V_{DS} = 10\text{ V}$	$-V_{(P)GS}$		4 to 6 V
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 0; V_{GS} = 7\text{ V}$	C_{rs}	<	1,5 pF
Drain-source resistance (on) at $f = 1\text{ kHz}$ $V_{GS} = 0; I_D = 0$	$R_{DS(on)}$	<	220 Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = shield lead connected to case

Accessories: 56246 (distance disc).

Note: Drain and source are interchangeable

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Gate current	I_G	max.	10	mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}	-55 to +200		$^{\circ}\text{C}$
Junction temperature	T_j	max.	200	$^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	590	K/W
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CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

$$-V_{GS} = 20\text{ V}; V_{DS} = 0 \quad -I_{GSS} < 0.1\text{ nA}$$

Drain current

$$V_{DG} = 20\text{ V}; I_S = 0 \quad I_{DGO} < 0.1\text{ nA}$$

$$V_{DG} = 20\text{ V}; I_S = 0; T_{amb} = 150\text{ }^{\circ}\text{C} \quad I_{DGO} < 0.2\text{ }\mu\text{A}$$

Drain current ¹⁾

$$V_{DS} = 20\text{ V}; V_{GS} = 0 \quad I_{DSS} > 2\text{ mA}$$

Gate-source breakdown voltage

$$-I_G = 1.0\text{ }\mu\text{A}; V_{DS} = 0 \quad -V_{(BR)GS} > 30\text{ V}$$

Gate-source voltage

$$I_D = 10\text{ nA}; V_{DS} = 10\text{ V} \quad -V_{(P)GS} \quad 4\text{ to }6\text{ V}$$

Drain-source voltage

$$I_D = 1.0\text{ mA}; V_{GS} = 0 \quad V_{DS} < 0.25\text{ V}$$

Drain cut-off current

$$V_{DS} = 10\text{ V}; -V_{GS} = 7.0\text{ V} \quad I_D < 1.0\text{ nA}$$

$$V_{DS} = 10\text{ V}; -V_{GS} = 7.0\text{ V}; T_{amb} = 150\text{ }^{\circ}\text{C} \quad I_D < 2.0\text{ }\mu\text{A}$$

Drain-source resistance (on) at $f = 1\text{ kHz}$

$$V_{GS} = 0; I_D = 0 \quad R_{DS(on)} < 220\text{ }\Omega$$

Input capacitance at $f = 1\text{ MHz}$

$$V_{DS} = 20\text{ V}; V_{GS} = 0 \quad C_{is} < 6\text{ pF}$$

Feedback capacitance at $f = 1\text{ MHz}$

$$V_{DS} = 0; V_{GS} = 7\text{ V} \quad -C_{rs} < 1.5\text{ pF}$$

Switching times

$$V_{DD} = 1.5\text{ V}; I_{D\text{ on}} = 1.0\text{ mA}$$

$$V_{GS\text{ on}} = 0; -V_{GS\text{ off}} = 6\text{ V}$$

$$\text{delay time} \quad t_d < 20\text{ ns}$$

$$\text{rise time} \quad t_r < 100\text{ ns}$$

$$\text{turn off time} \quad t_{off} < 100\text{ ns}$$

CHARACTERISTICS (continued)

Switching times

$$V_{DD} = 1.5 \text{ V}; I_{D \text{ on}} = 1.0 \text{ mA}$$

$$V_{GS \text{ on}} = 0; -V_{GS \text{ off}} = 6 \text{ V}$$

delay time	t_d	<	20	ns
rise time	t_r	<	100	ns
turn off time	t_{off}	<	100	ns

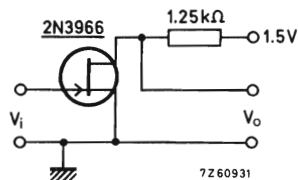


Fig. 2 Test circuit

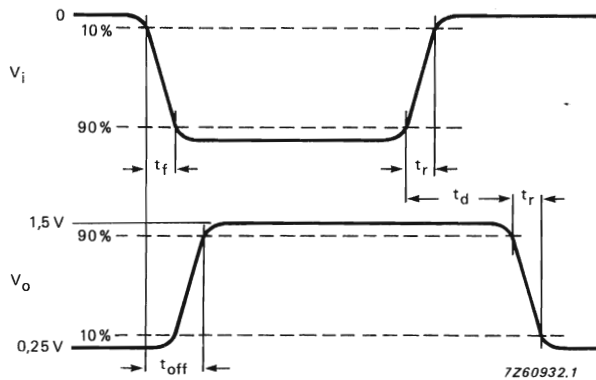


Fig. 3 Waveforms

Pulse generator:

$$\begin{aligned} t_r &< 1.0 \text{ ns} \\ t_f &< 1.0 \text{ ns} \\ t_p &= 1.0 \mu\text{s} \\ \delta &< 0.5 \\ R_S &= 50 \Omega \end{aligned}$$

Oscilloscope:

$$\begin{aligned} t_r &< 10 \text{ ns} \\ R_i &> 5 \text{ M}\Omega \\ C_i &< 10 \text{ pF} \end{aligned}$$

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power switching applications in industrial service.

QUICK REFERENCE DATA

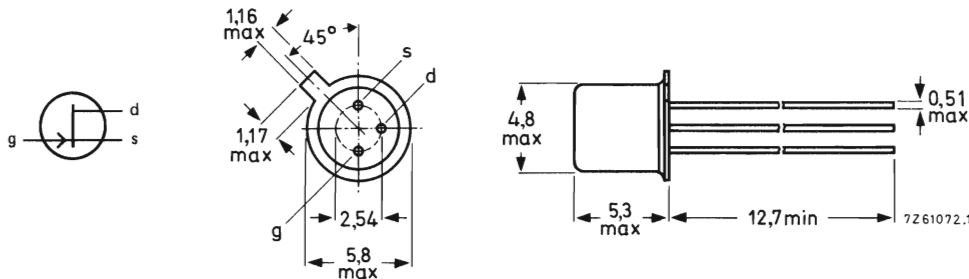
Drain-source voltage	$\pm V_{DS}$	max.	40	V	
Total power dissipation up to $T_{case} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max	1,8	W	
Drain current			2N4091	2N4092	2N4093
$V_{DS} = 20\text{ V}; V_{GS} = 0$	I_{DSS}	>	30	15	8 mA
Gate-source cut-off voltage					
$I_D = 1\text{ nA}; V_{DS} = 20\text{ V}$	$-V_{(P)GS}$	>	5,0	2,0	1,0 V
		<	10	7,0	5,0 V
Drain-source resistance (on) at $f = 1\text{ kHz}$					
$I_D = 0; V_{GS} = 0$	$r_{ds\text{ on}}$	<	30	50	80 Ω
Feedback capacitance at $f = 1\text{ MHz}$					
$V_{DS} = 0; -V_{GS} = 20\text{ V}$	C_{rs}	<	5,0		pF
Turn-off time					
$V_{DD} = 3,0\text{ V}; V_{GS} = 0$					
$I_D = 6,6\text{ mA}; -V_{GSM} = 12\text{ V}$	2N4091	t_{off}	<	40	ns
$I_D = 4,0\text{ mA}; -V_{GSM} = 8\text{ V}$	2N4092	t_{off}	<	60	ns
$I_D = 2,5\text{ mA}; -V_{GSM} = 6\text{ V}$	2N4093	t_{off}	<	80	ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case



Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V

Current

Forward gate current (d.c.)	I_G	max.	10	mA
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Total power dissipation up to $T_{case} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	1.8	W
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Storage temperature	T_{stg}	-55 to +200	$^{\circ}\text{C}$
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Junction temperature	T_j	max.	200	$^{\circ}\text{C}$
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THERMAL RESISTANCE

→ From junction to case in free air	$R_{th\ j-c}$	=	100	K/W
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CHARACTERISTICS

$T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified

Drain currents

$V_{DG} = 20\text{ V}; I_S = 0$ $I_{DGO} < 0.2\text{ nA}$

$V_{DG} = 20\text{ V}; I_S = 0; T_{amb} = 150^{\circ}\text{C}$ $I_{DGO} < 0.4\text{ }\mu\text{A}$

Source current

$V_{SG} = 20\text{ V}; I_D = 0$ $I_{SGO} < 0.2\text{ nA}$

Drain cut-off current

		2N4091	2N4092	2N4093
$V_{DS} = 20\text{ V}; -V_{GS} = 12\text{ V}$	$I_{DSX} <$	0.2	—	— nA
$V_{DS} = 20\text{ V}; -V_{GS} = 8\text{ V}$	$I_{DSX} <$	—	0.2	— nA
$V_{DS} = 20\text{ V}; -V_{GS} = 6\text{ V}$	$I_{DSX} <$	—	—	0.2 nA
$V_{DS} = 20\text{ V}; -V_{GS} = 12\text{ V}; T_{amb} = 150^{\circ}\text{C}$	$I_{DSX} <$	0.4	—	— μA
$V_{DS} = 20\text{ V}; -V_{GS} = 8\text{ V}; T_{amb} = 150^{\circ}\text{C}$	$I_{DSX} <$	—	0.4	— μA
$V_{DS} = 20\text{ V}; -V_{GS} = 6\text{ V}; T_{amb} = 150^{\circ}\text{C}$	$I_{DSX} <$	—	—	0.4 μA

Gate-source breakdown voltage

$-I_G = 1.0\text{ }\mu\text{A}; V_{DS} = 0$ $-V_{(BR)GSS} > 40\text{ V}$

Drain current ¹⁾

$V_{DS} = 20\text{ V}; V_{GS} = 0$ $I_{DSS} > 30\text{ mA}$

Gate-source cut-off voltage

$I_D = 1\text{ nA}; V_{DS} = 20\text{ V}$ $-V_{(P)GS} > 5.0\text{ V}$
 $-V_{(P)GS} < 10\text{ V}$

Drain-source voltages (on)

$I_D = 6.6\text{ mA}; V_{GS} = 0$ $V_{DSon} < 0.2\text{ V}$

$I_D = 4.0\text{ mA}; V_{GS} = 0$ $V_{DSon} < 0.2\text{ V}$

$I_D = 2.5\text{ mA}; V_{GS} = 0$ $V_{DSon} < 0.2\text{ V}$

Drain-source resistance (on)

$I_D = 1.0\text{ mA}; V_{GS} = 0$ $r_{DSon} < 30\text{ }\Omega$

Drain-source resistance (on) at $f = 1\text{ kHz}$

$I_D = 0; V_{GS} = 0$ $r_{ds\text{ on}} < 30\text{ }\Omega$

¹⁾ Measured under pulsed conditions: $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.03$

CHARACTERISTICS (continued)

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specifiedy-parameters at $f = 1\text{ MHz}$ (common source)

Input capacitance

$V_{DS} = 20\text{ V} ; V_{GS} = 0$

$C_{is} < 16\text{ pF}$

Feedback capacitance

$V_{DS} = 0 ; -V_{GS} = 20\text{ V}$

$C_{rs} < 5\text{ pF}$

Switching times

$V_{DD} = 3,0\text{ V} ; V_{GS} = 0$

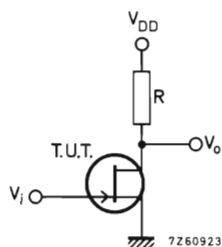
Delay time

Rise time

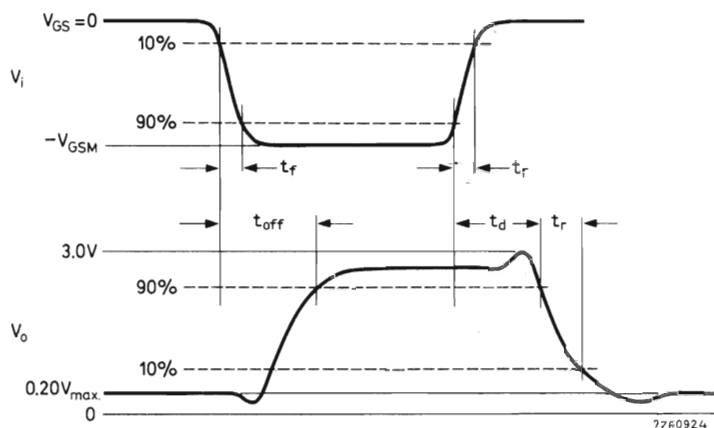
Turn-off time

		2N4091	2N4092	2N4093	
I_D	=	6,6	4,0	2,5	mA
$-V_{GSM}$	=	12	8	6	V
Delay time	t_d	< 15	15	20	ns
Rise time	t_r	< 10	20	40	ns
Turn-off time	t_{off}	< 40	60	80	ns

Test circuit:



$$R = \frac{2,8}{I_D}$$



Pulse generator:

t_r	<	1	ns
t_f	<	1	ns
t_p	=	1,0	μs
δ	=	0,1	
R_S	=	50	Ω

Oscilloscope:

t_r	<	0,4	ns
R_i	>	9,8	$\text{M}\Omega$
C_i	<	1,7	pF

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, application in industrial service.

QUICK REFERENCE DATA

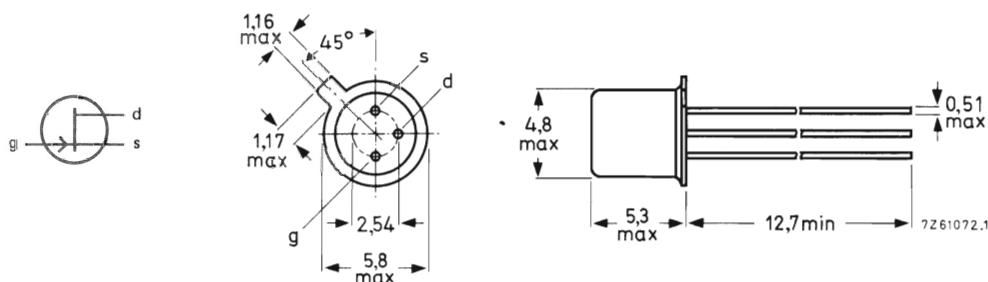
Drain-source voltage	$\pm V_{DS}$	max.	40	V		
Total power dissipation up to $T_{case} = 25^{\circ}C$	P_{tot}	max.	1,8	W		
Drain current			2N4391	2N4392	2N4393	
$V_{DS} = 20\text{ V}; V_{GS} = 0$	I_{DSS}	>	50	25	5 mA	
Gate-source cut-off voltage						
$I_D = 1\text{ nA}; V_{DS} = 20\text{ V}$	$-V_{(P)GS}$	>	4,0	2,0	0,5 V	
		<	10	5,0	3,0 V	
Drain-source resistance (on) at $f = 1\text{ kHz}$						
$I_D = 1\text{ mA}; V_{GS} = 0$	$r_{ds\ on}$	<	30	60	100 Ω	
Feedback capacitance at $f = 1\text{ MHz}$						
$V_{DS} = 0; -V_{GS} = 12\text{ V}$	2N4391 2N4392 2N4393	C_{rs}	<	3,5	3,5	3,5 pF
$V_{DS} = 0; -V_{GS} = 7\text{ V}$						
$V_{DS} = 0; -V_{GS} = 5\text{ V}$						
Turn-off time						
$V_{DD} = 10\text{ V}; V_{GS} = 0$						
$I_D = 12\text{ mA}; -V_{GSM} = 12\text{ V}$	t_{off}	<	20	—	—	ns
$I_D = 6,0\text{ mA}; -V_{GSM} = 7\text{ V}$	t_{off}	<	—	35	—	ns
$I_D = 3,0\text{ mA}; -V_{GSM} = 5\text{ V}$	t_{off}	<	—	—	50	ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case



Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate current (d.c.)	I_G	max.	50	mA
Total power dissipation up to $T_{case} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	1.8	W
Storage temperature	T_{stg}	-65 to	200	$^{\circ}\text{C}$
Junction temperature	T_j	max.	200	$^{\circ}\text{C}$
→ From junction to case in free air	$R_{th\ j-c}$	=	100	K/W

CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off current

$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS} <$	0.1	nA
$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_{amb} = 150\text{ }^{\circ}\text{C}$	$-I_{GSS} <$	0.2	μA

Drain cut-off current

		2N4391	2N4392	2N4393
$V_{DS} = 20\text{ V}; -V_{GS} = 12\text{ V}$	$I_{DSX} <$	0.1	-	- nA
$V_{DS} = 20\text{ V}; -V_{GS} = 7\text{ V}$	$I_{DSX} <$	-	0.1	- nA
$V_{DS} = 20\text{ V}; -V_{GS} = 5\text{ V}$	$I_{DSX} <$	-	-	0.1 nA
$V_{DS} = 20\text{ V}; -V_{GS} = 12\text{ V}; T_{amb} = 150\text{ }^{\circ}\text{C}$	$I_{DSX} <$	0.2	-	- μA
$V_{DS} = 20\text{ V}; -V_{GS} = 7\text{ V}; T_{amb} = 150\text{ }^{\circ}\text{C}$	$I_{DSX} <$	-	0.2	- μA
$V_{DS} = 20\text{ V}; -V_{GS} = 5\text{ V}; T_{amb} = 150\text{ }^{\circ}\text{C}$	$I_{DSX} <$	-	-	0.2 μA

CHARACTERISTICS (continued)

 $T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified

		2N4391	2N4392	2N4393
Drain currents ¹⁾				
$V_{DS} = 20\text{ V}; V_{GS} = 0$	$I_{DSS} >$	50	—	— mA
	$I_{DSS} <$	150	—	— mA
$V_{DS} = 20\text{ V}; V_{GS} = 0$	$I_{DSS} >$	—	25	— mA
	$I_{DSS} <$	—	75	— mA
$V_{DS} = 20\text{ V}; V_{GS} = 0$	$I_{DSS} >$	—	—	5 mA
	$I_{DSS} <$	—	—	30 mA
Gate-source breakdown voltage				
$-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS} >$	40	40	40 V
Gate-source voltage				
$I_G = 1\text{ mA}; V_{DS} = 0$	$V_{GSon} <$	1.0	1.0	1.0 V
Gate-source cut-off voltage				
$I_D = 1\text{ nA}; V_{DS} = 20\text{ V}$	$-V_{(P)GS} >$	4.0	2.0	0.5 V
	$-V_{(P)GS} <$	10	5.0	3.0 V
Drain-source voltage (on)				
$I_D = 12\text{ mA}; V_{GS} = 0$	$V_{DSon} <$	0.4	—	— V
$I_D = 6.0\text{ mA}; V_{GS} = 0$	$V_{DSon} <$	—	0.4	— V
$I_D = 3.0\text{ mA}; V_{GS} = 0$	$V_{DSon} <$	—	—	0.4 V
Drain-source resistance (on)				
$I_D = 1\text{ mA}; V_{GS} = 0$	$r_{DSon} <$	30	60	100 Ω
Drain-source resistance (on) at $f = 1\text{ kHz}$				
$I_D = 0; V_{GS} = 0$	$r_{dson} <$	30	60	100 Ω
y parameters at $f = 1\text{ MHz}$ (common source)				
Input capacitance				
$V_{DS} = 20\text{ V}; V_{GS} = 0$	$C_{is} <$	14	14	14 pF
Feedback capacitance				
$-V_{GS} = 12\text{ V}; V_{DS} = 0$	$-C_{rs} <$	3.5	—	— pF
$-V_{GS} = 7\text{ V}; V_{DS} = 0$	$-C_{rs} <$	—	3.5	— pF
$-V_{GS} = 5\text{ V}; V_{DS} = 0$	$-C_{rs} <$	—	—	3.5 pF

¹⁾ measured under pulsed conditions: $t_p = 100\text{ }\mu\text{s}; \delta = 0.01$

CHARACTERISTICS (continued)

 $T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified

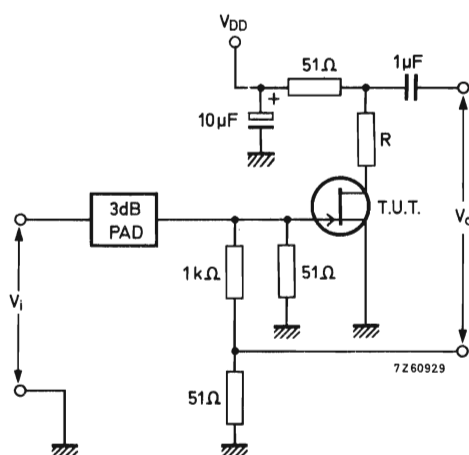
Switching times

$V_{DD} = 10\text{ V}; V_{GS} = 0$

Rise time
Turn on time
Fall time
Turn off time

	2N4391	2N4392	2N4393	
I_D	= 12	6.0	3.0	mA
$-V_{GSM}$	= 12	7	5	V
t_r	< 5	5	5	ns
t_{on}	< 15	15	15	ns
t_f	< 15	20	30	ns
t_{off}	< 20	35	50	ns

Test circuit:



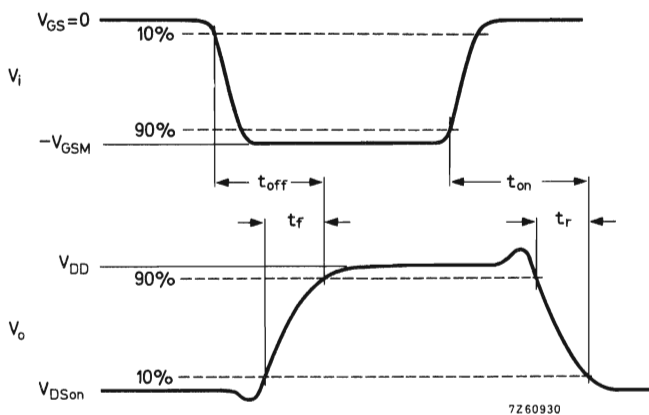
$$R = \frac{9.6}{I_D} - 51\Omega$$

Pulse generator:

$$\begin{aligned} t_r &< 0.5 \text{ ns} \\ t_f &< 0.5 \text{ ns} \\ t_p &= 100 \mu\text{s} \\ \delta &= 0.01 \end{aligned}$$

Oscilloscope:

$$R_i = 50 \Omega$$



N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, applications in industrial service.

QUICK REFERENCE DATA

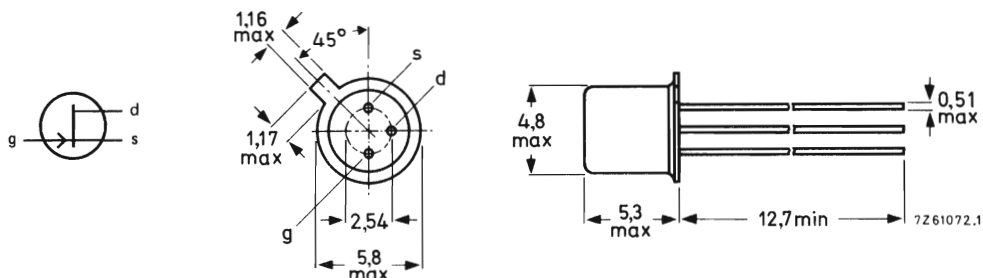
Drain-source voltage	2N4856 to 2N4858 2N4859 to 2N4861	$\pm V_{DS}$ $\pm V_{DS}$	max. max.	40 30	V V	
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$		P_{tot}	max.	360	mW	
Drain current				2N4856 2N4859	2N4857 2N4860	2N4858 2N4861
$V_{DS} = 15\text{ V}; V_{GS} = 0$		I_{DSS}	$>$	50	20	8 mA
Gate-source cut-off voltage						
$I_D = 0,5\text{ nA}; V_{DS} = 15\text{ V}$		$-V_{(P)GS}$	$>$ $<$	4 10	2 6	0,8 V 4 V
Drain-source resistance (on) at $f = 1\text{ kHz}$						
$I_D = 0; V_{GS} = 0$		$r_{ds\ on}$	$<$	25	40	60 Ω
Feedback capacitance at $f = 1\text{ MHz}$						
$V_{DS} = 0; -V_{GS} = 10\text{ V}$		C_{rs}	$<$	8		pF
Turn-off time						
$V_{DD} = 10\text{ V}; V_{GS} = 0$						
$I_D = 20\text{ mA}; -V_{GSM} = 10\text{ V}$	2N4856; 2N4859	t_{off}	$<$	25		ns
$I_D = 10\text{ mA}; -V_{GSM} = 6\text{ V}$	2N4857; 2N4860	t_{off}	$<$	50		ns
$I_D = 5\text{ mA}; -V_{GSM} = 4\text{ V}$	2N4858; 2N4861	t_{off}	$<$	100		ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18

Gate connected to case



Accessories: 56246 (distance disc).

Note: Drain and source are interchangeable.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

		2N4856	2N4859	
		2N4857	2N4860	
		2N4858	2N4861	
Drain-source voltage	$\pm V_{DS}$	max. 40	30	V
Drain-gate voltage (open source)	V_{DGO}	max. 40	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max. 40	30	V
Gate current (d.c.)	I_G	max.	50	mA
Total power dissipation up to $T_{amb} = 25^{\circ}C$	P_{tot}	max.	360	mW
Storage temperature	T_{stg}	-65 to +200		$^{\circ}C$
Junction temperature	T_j	max.	200	$^{\circ}C$
THERMAL RESISTANCE				
→ From junction to ambient in free air	$R_{th\ j-a}$	=	490	K/W

CHARACTERISTICS

$T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

		2N4856	2N4857	2N4858	2N4859	2N4860	2N4861
$-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS} <$	0.25	-	-	-	-	nA
$-V_{GS} = 15\text{ V}; V_{DS} = 0$	$-I_{GSS} <$	-	0.25	-	-	-	nA
$-V_{GS} = 20\text{ V}; V_{DS} = 0; T_{amb} = 150^{\circ}\text{C}$	$-I_{GSS} <$	0.5	-	-	-	-	μA
$-V_{GS} = 15\text{ V}; V_{DS} = 0; T_{amb} = 150^{\circ}\text{C}$	$-I_{GSS} <$	-	0.5	-	-	-	μA

Drain cut-off current

$V_{DS} = 15\text{ V}; -V_{GS} = 10\text{ V}$	$I_{DSX} <$	0.25	0.25	nA
$V_{DS} = 15\text{ V}; -V_{GS} = 10\text{ V}; T_{amb} = 150^{\circ}\text{C}$	$I_{DSX} <$	0.5	0.5	μA

Drain current ¹⁾

		2N4856	2N4857	2N4858	2N4859	2N4860	2N4861
$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS} >$	50	20	8	50	20	8
	$I_{DSS} <$	-	100	80	-	100	80

Gate-source breakdown voltage

		2N4856	2N4857	2N4858	2N4859	2N4860	2N4861
$-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	40	30	30	40	30	30

Gate-source cut-off voltage

		2N4856	2N4857	2N4858	2N4859	2N4860	2N4861
$I_D = 0.5\text{ nA}; V_{DS} = 15\text{ V}$	$-V_{(P)GS} >$	4	2	0.8	4	2	0.8
	$-V_{(P)GS} <$	10	6	4	10	6	4

Drain-source voltage (on)

$I_D = 20\text{ mA}; V_{GS} = 0$	$V_{DSon} <$	0.75	-	-	0.75	-	-
$I_D = 10\text{ mA}; V_{GS} = 0$	$V_{DSon} <$	-	0.50	-	-	0.50	-
$I_D = 5\text{ mA}; V_{GS} = 0$	$V_{DSon} <$	-	-	0.50	-	-	0.50

Drain-source resistance (on) at $f = 1\text{ kHz}$

$I_D = 0; V_{GS} = 0$	$r_{dson} <$	25	40	60	25	40	60
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¹⁾ measured under pulsed conditions: $t_p = 100\text{ ms}; \delta \leq 0.1$

y-parameters (common source)

$V_{DS} = 0$; $-V_{GS} = 10 \text{ V}$; $f = 1 \text{ MHz}$

Input capacitance

$C_{is} < \begin{matrix} 18 \\ 8 \end{matrix} \text{ pF}$

Feedback capacitance

$C_{rs} < \begin{matrix} 18 \\ 8 \end{matrix} \text{ pF}$

Switching times (see Figs 2 and 3)

$V_{DD} = 10 \text{ V}$; $V_{GS} = 0$

Drain current

$I_D = \begin{matrix} 20 \\ 10 \\ 5 \end{matrix} \text{ mA}$

Gate-source voltage (peak value)

$-V_{GSM} = \begin{matrix} 10 \\ 6 \\ 4 \end{matrix} \text{ V}$

Delay time

$t_d < \begin{matrix} 6 \\ 6 \\ 10 \end{matrix} \text{ ns}$

Rise time

$t_r < \begin{matrix} 3 \\ 4 \\ 10 \end{matrix} \text{ ns}$

Turn-off time

$t_{off} < \begin{matrix} 25 \\ 50 \\ 100 \end{matrix} \text{ ns}$

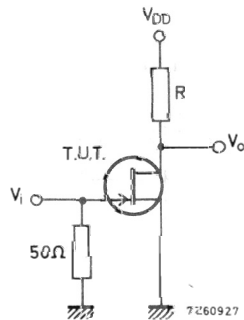


Fig. 2 Switching times test circuit.

2N4856	2N4857	2N4858
2N4859	2N4860	2N4861
R = 464	953	1910 Ω

Pulse generator:

$t_r \leq 1 \text{ ns}$

$t_f \leq 1 \text{ ns}$

$\delta = 0,02$

$Z_o = 50 \Omega$

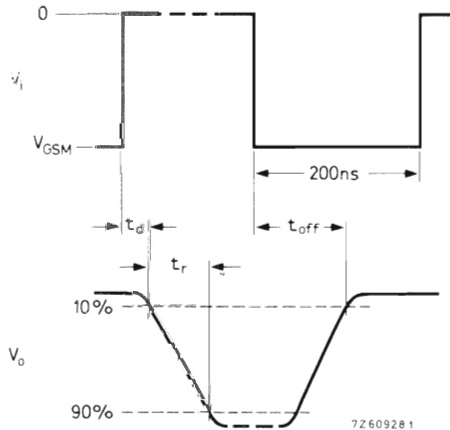


Fig. 3 Input and output waveforms.

Oscilloscope:

$t_r \leq 0,75 \text{ ns}$

$R_i \geq 1 \text{ M}\Omega$

$C_i \leq 2,5 \text{ pF}$

DEVICE DATA

MOS-FETS

single gate

N-CHANNEL INSULATED GATE MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for linear applications in the audio as well as the i.f. and v.h.f. frequency region, and in cases where high input impedance, low gate leakage currents and low noise figures are of importance.

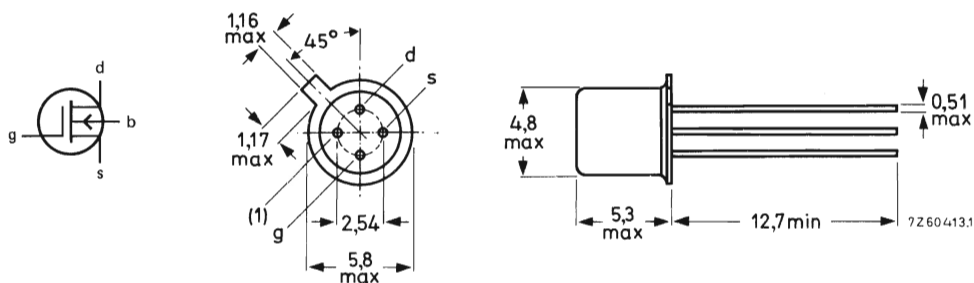
QUICK REFERENCE DATA

Drain-substrate voltage	V_{DB}	max.	30 V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10 V
Drain current $V_{DS} = 15 \text{ V}; V_{GS} = 0$	I_{DSS}		10 to 40 mA
Transfer admittance $I_D = 5 \text{ mA}; V_{DS} = 15 \text{ V}; f = 1 \text{ kHz}$	$ Y_{fs} $	>	6 mS
Feedback capacitance $I_D = 5 \text{ mA}; V_{DS} = 15 \text{ V}; f = 1 \text{ MHz}$	C_{rs}	<	0,7 pF
Noise figure at $f = 200 \text{ MHz}$ $I_D = 5 \text{ mA}; V_{DS} = 15 \text{ V}; T_{amb} = 25^\circ\text{C}$ $G_S = 1 \text{ mS}; B_S = B_{Sopt}$	F	<	5 dB
Equivalent noise voltage at $f = 1 \text{ kHz}$ $I_D = 5 \text{ mA}; V_{DS} = 15 \text{ V}; T_{amb} = 25^\circ\text{C}$	V_n/\sqrt{B}	typ.	100 nV/ $\sqrt{\text{Hz}}$

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = substrate (b) connected to case

Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-substrate voltage	V_{DB}	max.	30 V
Source-substrate voltage	V_{SB}	max.	30 V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10 V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	V_{G-N}	max.	15 V
		min.	-15 V
Drain current (d.c.)	I_D	max.	20 mA
Drain current (peak value) $t_p = 20$ ms; $\delta = 0,1$	I_{DM}	max.	50 mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	200 mW
Storage temperature	T_{stg}	-65 to + 125 °C	
Junction temperature	T_j	max.	125 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	500 K/W
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CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specifiedGate currents; $V_{BS} = 0$ $-V_{GS} = 10\text{ V}; V_{DS} = 0$ $-I_{GSS} < 10\text{ pA}$ $V_{GS} = 10\text{ V}; V_{DS} = 0$ $I_{GSS} < 10\text{ pA}$ $-V_{GS} = 10\text{ V}; V_{DS} = 0; T_j = 125^\circ\text{C}$ $-I_{GSS} < 200\text{ pA}$ $V_{GS} = 10\text{ V}; V_{DS} = 0; T_j = 125^\circ\text{C}$ $I_{GSS} < 200\text{ pA}$ Bulk currents; $V_{GB} = 0$ $-V_{BD} = 30\text{ V}; I_S = 0$ $-I_{BDO} < 10\text{ }\mu\text{A}$ $-V_{BS} = 30\text{ V}; I_D = 0$ $-I_{BSO} < 10\text{ }\mu\text{A}$

Drain current

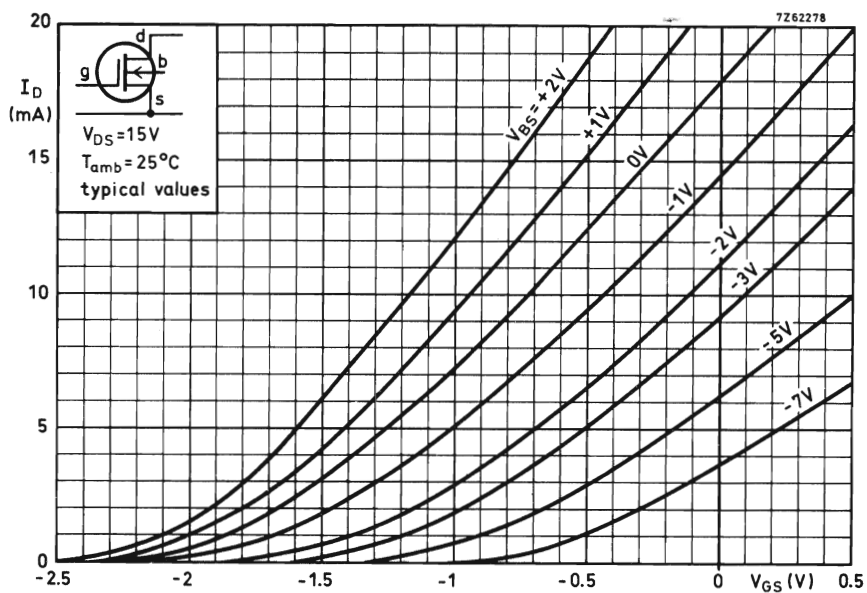
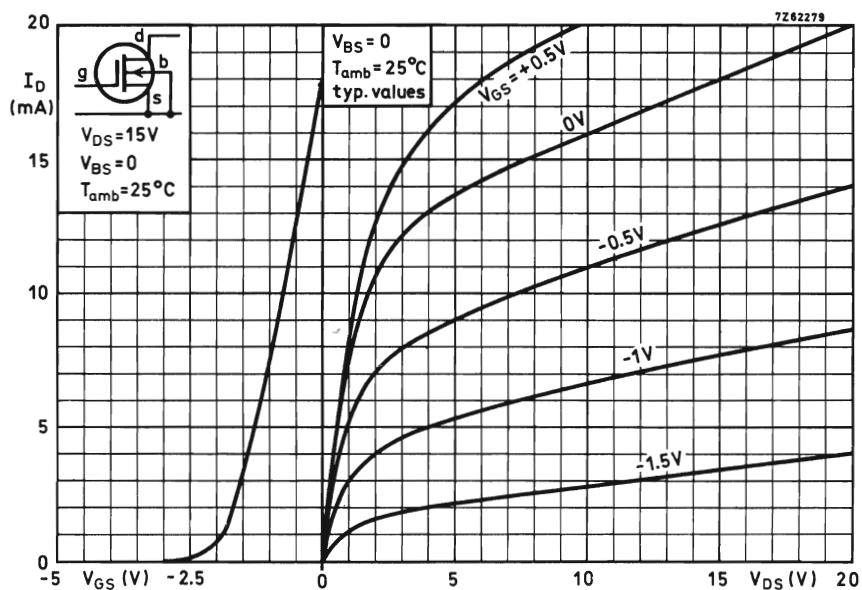
 $V_{DS} = 15\text{ V}; V_{GS} = 0$ $I_{DSS} \quad 10\text{ to }40\text{ mA}$

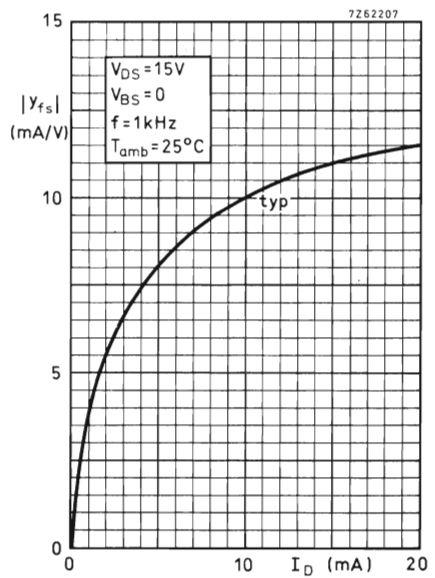
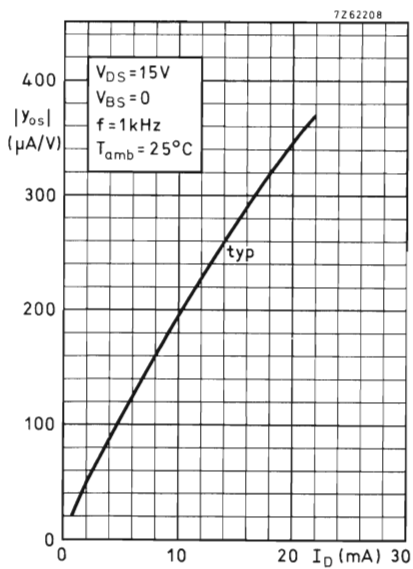
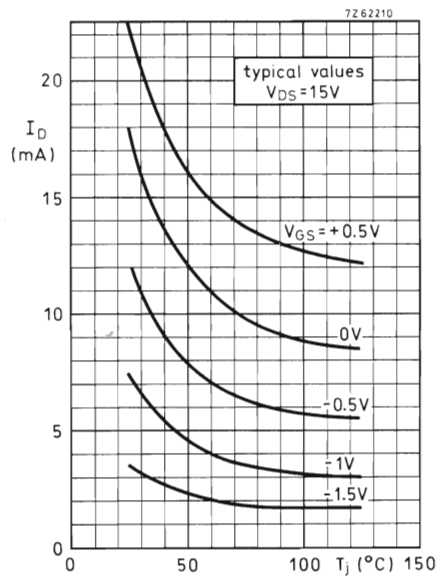
Gate-source voltage

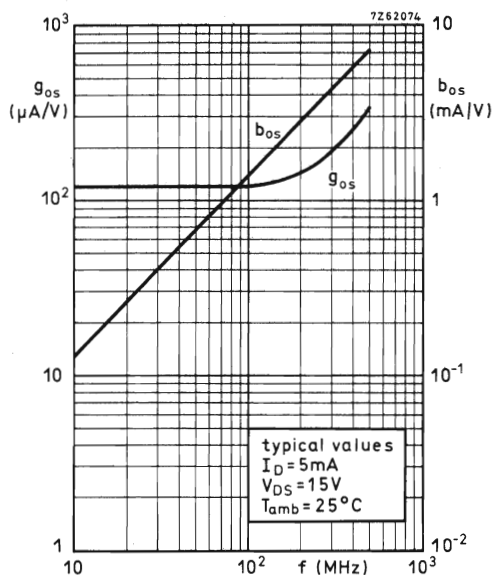
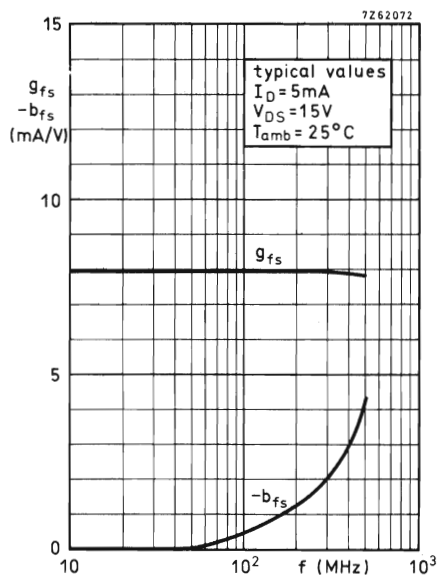
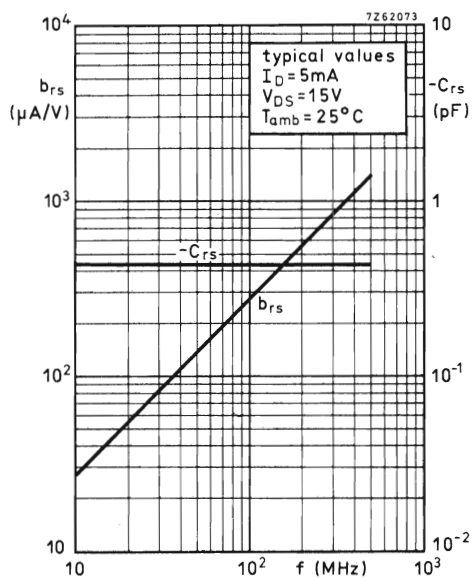
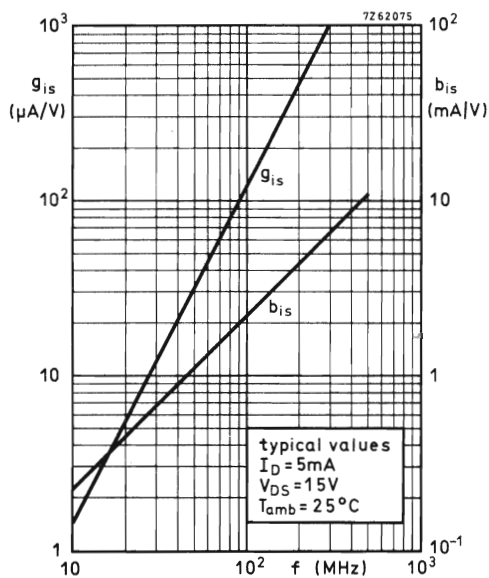
 $I_D = 100\text{ nA}; V_{DS} = 15\text{ V}$ $-V_{GS} \quad 0.5\text{ to }3.5\text{ V}$

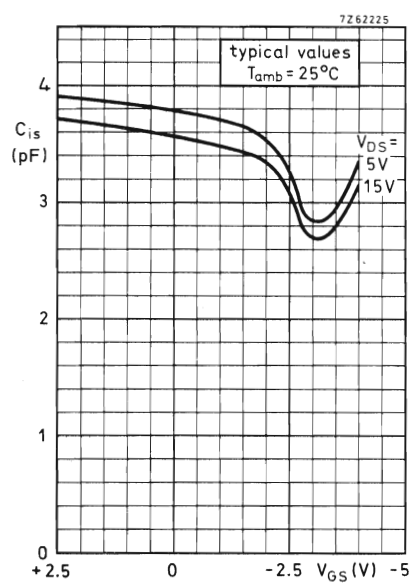
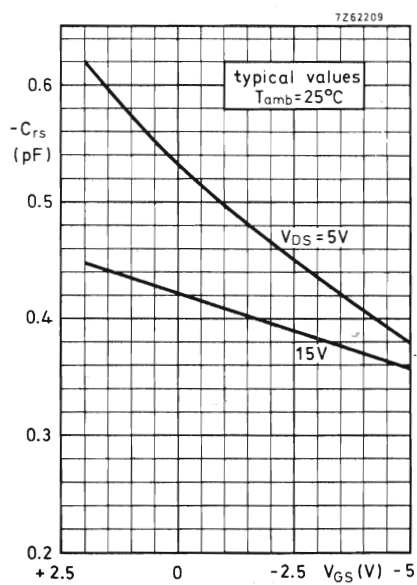
Gate-source cut-off voltage

 $I_D = 100\text{ nA}; V_{DS} = 15\text{ V}$ $-V_{(P)GS} < 4\text{ V}$ y parameters $T_{amb} = 25^\circ\text{C}$ $I_D = 5\text{ mA}; V_{DS} = 15\text{ V}$ Transfer admittance at $f = 1\text{ kHz}$ $|Y_{fs}| > 6\text{ mS}$ Output admittance at $f = 1\text{ kHz}$ $|Y_{os}| < 0.4\text{ mS}$ Input capacitance at $f = 1\text{ MHz}$ $C_{is} < 5\text{ pF}$ Feedback capacitance at $f = 1\text{ MHz}$ $C_{rs} < 0.7\text{ pF}$ Output capacitance at $f = 1\text{ MHz}$ $C_{os} < 3\text{ pF}$ Noise figure at $f = 200\text{ MHz}$ $T_{amb} = 25^\circ\text{C}$ $I_D = 5\text{ mA}; V_{DS} = 15\text{ V}$ $G_S = 1\text{ mS}; B_S = B_{Sopt}$ $F < 5\text{ dB}$ Equivalent noise voltage $T_{amb} = 25^\circ\text{C}$ $I_D = 5\text{ mA}; V_{DS} = 15\text{ V}; f = 120\text{ Hz}$ $V_n/\sqrt{B} \quad \text{typ. } 300\text{ nV}/\sqrt{\text{Hz}}$ $f = 1\text{ kHz}$ $V_n/\sqrt{B} \quad \text{typ. } 100\text{ nV}/\sqrt{\text{Hz}}$ $f = 10\text{ kHz}$ $V_n/\sqrt{B} \quad \text{typ. } 35\text{ nV}/\sqrt{\text{Hz}}$









MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTORS

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel depletion mode type.

The transistor is sealed in a TO-72 envelope and features a low ON-resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver
- convertor
- chopper

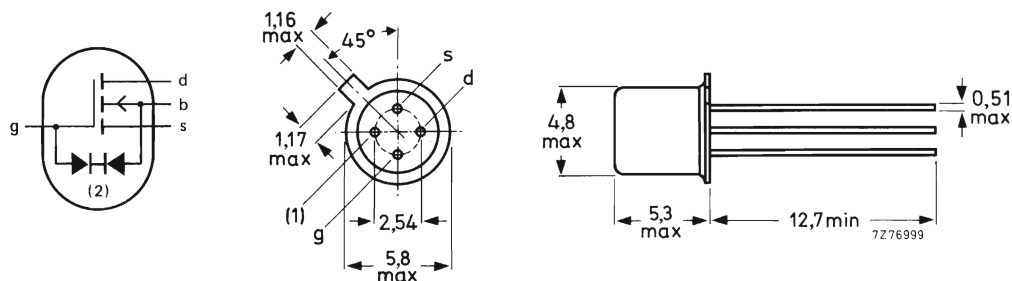
QUICK REFERENCE DATA

			BSD10	BSD12
Drain-source voltage	V_{DS}	max.	10	20 V
Gate-source voltage	V_{GS}	max.	+15 -30	+15 V -40 V
Drain current (d.c.)	I_D	max.	50	mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$ (free air)	P_{tot}	max.	275	mW
Junction temperature	T_j	max.	125	$^{\circ}\text{C}$
Drain-source ON-resistance $V_{GS} = 10\text{ V}$; $V_{SB} = 0$; $I_D = 1\text{ mA}$	R_{DSon}	<	30	Ω
Feedback capacitance $V_{GS} = V_{BS} = -5\text{ V}$; $V_{DS} = 10\text{ V}$; $f = 1\text{ MHz}$	C_{rss}	typ.	0,6	pF

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) Substrate (b) connected to case.

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD10	BSD12
Drain-source voltage	V_{DS}	max.	10	20 V
Source-drain voltage	V_{SD}	max.	10	20 V
Drain-substrate voltage	V_{DB}	max.	15	25 V
Source-substrate voltage	V_{SB}	max.	15	25 V
Gate-substrate voltage	V_{GB}	max.	+15 -15	+15 V -15 V
Gate-source voltage	V_{GS}	max.	+15 -30	+15 V -40 V
Drain current (d.c.)	I_D	max.	50	mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$ in free air	P_{tot}	max.	275	mW
Storage temperature	T_{stg}		-65 to +150	$^{\circ}\text{C}$
Junction temperature	T_j	max.	125	$^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	360	K/W
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CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

			BSD10	BSD12
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5\text{ V}$; $I_S = 10\text{ nA}$	$V_{(BR)DSX}$	>	10	20 V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5\text{ V}$; $I_D = 10\text{ nA}$	$V_{(BR)SDX}$	>	10	20 V
Drain-substrate breakdown voltage $V_{GB} = 0$; $I_D = 10\text{ nA}$; open source	$V_{(BR)DBO}$	>	15	25 V
Source-substrate breakdown voltage $V_{GB} = 0$; $I_S = 10\text{ nA}$; open drain	$V_{(BR)SBO}$	>	15	25 V
Drain-source leakage current $V_{GS} = V_{BS} = -5\text{ V}$; $V_{DS} = 10\text{ V}$	I_{DSoff}	typ.	1,0	nA
Source-drain leakage current $V_{GD} = V_{BD} = -5\text{ V}$; $V_{SD} = 10\text{ V}$	I_{SDoff}	typ.	1,0	nA
Gate-substrate leakage current $V_{DB} = V_{SB} = 0$; $V_{GB} = \pm 15\text{ V}$	I_{GBS}	<	10	nA
Forward transconductance at $f = 1\text{ kHz}$ $V_{DS} = 10\text{ V}$; $V_{SB} = 0$; $I_S = 20\text{ mA}$	g_{fs}	> typ.	10 15	mS mS

Gate-source cut-off voltage

$$V_{DS} = 10 \text{ V}; V_{SB} = 0;$$

$$I_D = 10 \mu\text{A}$$

Drain-source ON-resistance

$$I_D = 1 \text{ mA}; V_{SB} = 0$$

$$V_{GS} = 5 \text{ V}$$

$$V_{GS} = 10 \text{ V}$$

Capacitances at $f = 1 \text{ MHz}$ (see Fig. 2)

$$V_{GS} = V_{BS} = -5 \text{ V}; V_{DS} = 10 \text{ V}$$

Feed-back capacitance

Input capacitance

Output capacitance

Switching times (see Fig. 3)

$$V_{DD} = 10 \text{ V}; V_i = -5 \text{ to } +5 \text{ V}$$

$$-V_{(P)GS} < 2,0 \text{ V}$$

$$r_{DSon} \text{ typ. } 25 \Omega$$

$$< 50 \Omega$$

$$r_{DSon} \text{ typ. } 15 \Omega$$

$$< 30 \Omega$$

$$C_{rss} \text{ typ. } 0,6 \text{ pF}$$

$$C_{iss} \text{ typ. } 2,3 \text{ pF}$$

$$C_{oss} \text{ typ. } 1,9 \text{ pF}$$

$$t_{on} \text{ typ. } 1,0 \text{ ns}$$

$$t_{off} \text{ typ. } 5,0 \text{ ns}$$

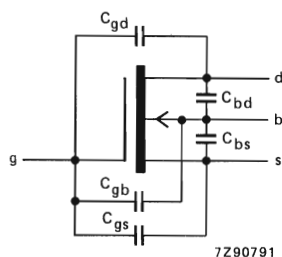
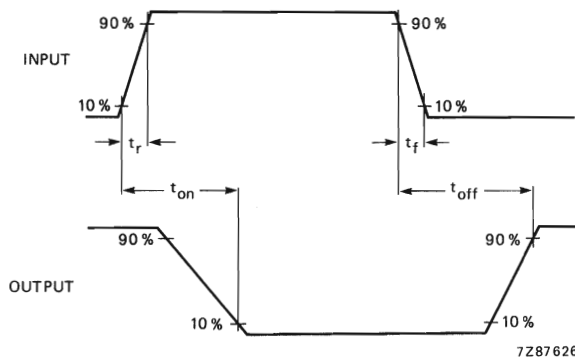
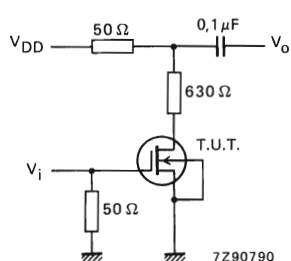


Fig. 2 Capacitances model.

$$C_{iss} = C_{gs} + C_{gd} + C_{gb}$$

$$C_{oss} = C_{gd} + C_{bd}$$

$$C_{rss} = C_{gd}$$

Fig. 3 Switching times and input and output waveforms;
 $R_i = 50 \Omega$; $t_r < 0,5 \text{ ns}$; $t_f < 1,0 \text{ ns}$; $t_p = 20 \text{ ns}$; $\delta < 0,01$.

MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTORS

Symmetrical insulated-gate silicon MOS field-effect transistors of the N-channel depletion mode type. The transistor is sealed in a SOT-143 envelope and features a low ON-resistance and low capacitances. The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver
- convertor
- chopper

QUICK REFERENCE DATA

		BSD20	BSD22	
Drain-source voltage	V_{DS}	max. 10	20 V	
Gate-source voltage	V_{GS}	max. +15 -30	+15 V -40 V	←
Drain current (d.c.)	I_D	max. 50	mA	
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max. 230	mW	
Junction temperature	T_j	max. 125	$^{\circ}\text{C}$	
Drain-source ON-resistance $V_{GS} = 10\text{ V}; V_{SB} = 0; I_D = 1\text{ mA}$	R_{DSon}	< 30	Ω	
Feed-back capacitance $V_{GS} = V_{BS} = -5\text{ V}; V_{DS} = 10\text{ V}; f = 1\text{ MHz}$	C_{rss}	typ. 0,6	pF	

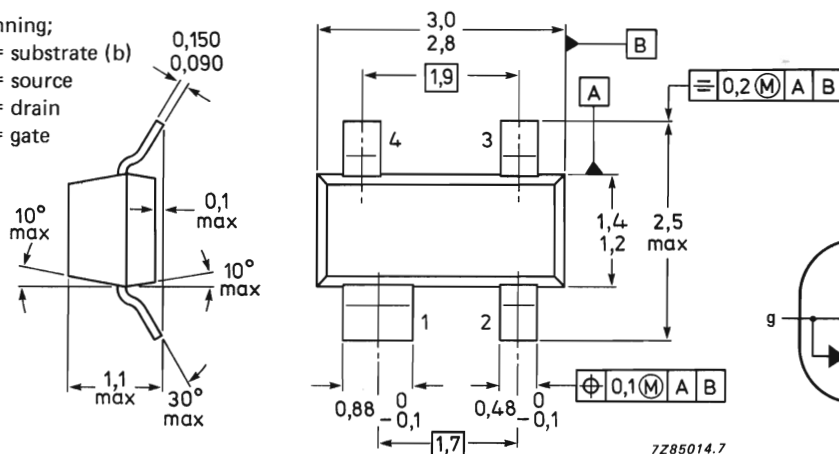
MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-143.

Pinning;

- 1 = substrate (b)
2 = source
3 = drain
4 = gate



TOP VIEW

Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD20	BSD22
Drain-source voltage	V_{DS}	max.	10	20 V
Source-drain voltage	V_{SD}	max.	10	20 V
Drain-substrate voltage	V_{DB}	max.	15	25 V
Source-substrate voltage	V_{SB}	max.	15	25 V
Gate-substrate voltage	V_{GB}	max.	± 15	± 25 V
Gate-source voltage	V_{GS}	max.	$+15$ -30	$+15$ -40 V
Drain current (d.c.)	I_D	max.	50	mA
Total power dissipation up to $T_{amb} = 25^\circ\text{C}^*$	P_{tot}	max.	230	mW
Storage temperature	T_{stg}		-65 to $+150$	$^\circ\text{C}$
Junction temperature	T_j	max.	125	$^\circ\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air*

$R_{th\ j-a}$	=	430	K/W
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CHARACTERISTICS

$T_{amb} = 25^\circ\text{C}$ unless otherwise specified

			BSD20	BSD22
Drain-source breakdown voltage				
$V_{GS} = V_{BS} = -5\text{ V}; I_S = 10\text{ nA}$	$V_{(BR)DSX}$	>	10	20 V
Source-drain breakdown voltage				
$V_{GD} = V_{BD} = -5\text{ V}; I_D = 10\text{ nA}$	$V_{(BR)SDX}$	>	10	20 V
Drain-substrate breakdown voltage				
$V_{GB} = 0; I_D = 10\text{ nA};$ open source	$V_{(BR)DBO}$	>	15	25 V
Source-substrate breakdown voltage				
$V_{GB} = 0; I_S = 10\text{ nA};$ open drain	$V_{(BR)SBO}$	>	15	25 V
Drain-source leakage current				
$V_{GS} = V_{BS} = -5\text{ V}; V_{DS} = 10\text{ V}$	I_{DSoff}	typ.	1,0	nA
Source-drain leakage current				
$V_{GD} = V_{BD} = 5\text{ V}; V_{SD} = 10\text{ V}$	I_{SDoff}	typ.	1,0	nA
Gate-substrate leakage current				
$\rightarrow V_{DB} = V_{SB} = 0; V_{GB} = \pm 15\text{ V}$	I_{GBS}	<	10	nA

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Forward transconductance at $f = 1$ kHz

$$V_{DS} = 10 \text{ V}; V_{SB} = 0; I_D = 20 \text{ mA}$$

g_{fs}	>	10 mS
	typ.	15 mS

Gate-source cut-off voltage

$$V_{DS} = 10 \text{ V}; V_{SB} = 0; I_D = 10 \mu\text{A}$$

$$I_D = 10 \mu\text{A}$$

$-V_{(P)GS}$	<	2,0 V
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Drain-source ON-resistance

$$I_D = 1 \text{ mA}; V_{SB} = 0;$$

$$V_{GS} = 5 \text{ V}$$

R_{DSon}	typ.	25 Ω
	<	50 Ω

$$V_{GS} = 10 \text{ V}$$

R_{DSon}	typ.	15 Ω
	<	30 Ω

Capacitances at $f = 1$ MHz

$$V_{GS} = V_{BS} = -5 \text{ V}; V_{DS} = 10 \text{ V}$$

Feed-back capacitance

Input capacitance

Output capacitance

C_{rss}	typ.	0,6 pF
-----------	------	--------

C_{iss}	typ.	1,5 pF
-----------	------	--------

C_{oss}	typ.	1,0 pF
-----------	------	--------

Switching times (see Fig. 3)

$$V_{DD} = 10 \text{ V}; V_i = -5 \text{ V to } +5 \text{ V}$$

t_{on}	typ.	1,0 ns
t_{off}	typ.	5,0 ns

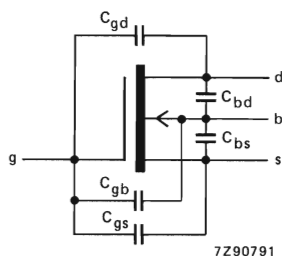


Fig. 2 Capacitances model.

$$C_{iss} = C_{gs} + C_{gd} + C_{gb}$$

$$C_{oss} = C_{gd} + C_{bd}$$

$$C_{rss} = C_{gd}$$

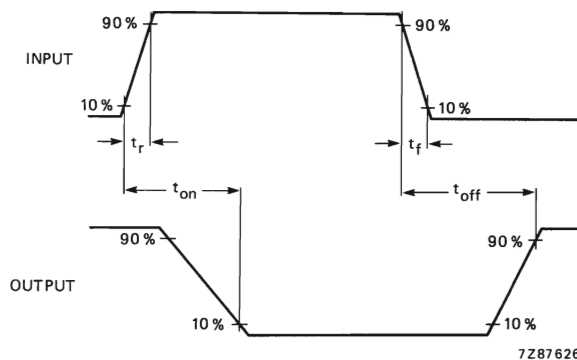
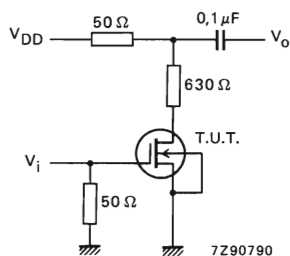


Fig. 3 Switching times and input and output waveforms;

$$R_i = 50 \Omega; t_r < 0,5 \text{ ns}; t_f < 1,0 \text{ ns}; t_p = 20 \text{ ns}; \delta < 0,01.$$

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTORS

Symmetrical insulated gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

These transistors are hermetically sealed in a TO-72 envelope and feature a low ON-resistance, high switching speed and low capacitances.

The types BSD213 and BSD215 are protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analogue and/or digital switch
- switch driver
- converters
- choppers

QUICK REFERENCE DATA

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Gate-source voltage	V_{GS}	max.	± 40	$+15$ -30	± 40	$+15$ -40	V
Drain current (d.c.)	I_D	max.	50				mA
Total power dissipation up to $T_{amb} = 25^\circ\text{C}$ (free air)	P_{tot}	max.	275				mW
Drain-source resistance $I_D = 1\text{ mA}; V_{SB} = 0; V_{GS} = 15\text{ V}$	$R_{DS(on)}$	typ.	25				Ω
Feedback capacitance $V_{GS} = V_{BS} = -15\text{ V};$ $V_{DS} = 10\text{ V}; f = 1\text{ MHz}$	C_{rss}	typ.	0,6				pF
Junction temperature	T_j	max.	125				$^\circ\text{C}$

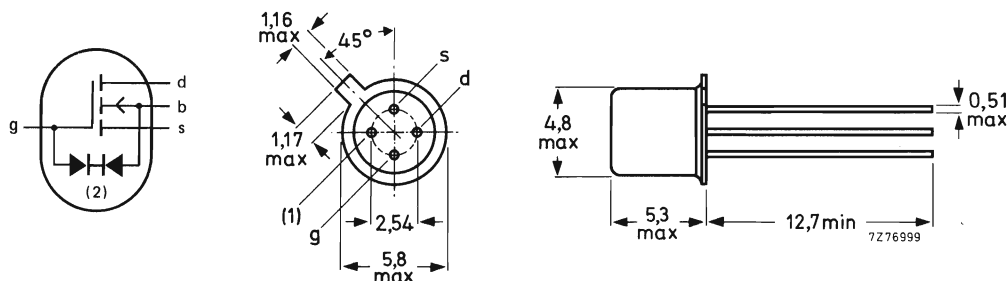
MECHANICAL DATA

See next page.

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



- (1) Substrate (b) connected to case.
(2) Diode protection on types BSD213 and BSD215 only.

BSD212 and BSD214 have no protection diode.

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Source-drain voltage	V_{SD}	max.	10	10	20	20	V
Drain-substrate voltage	V_{DB}	max.	15	15	25	25	V
Source-substrate voltage	V_{SB}	max.	15	15	25	25	V
Gate-substrate voltage	V_{GB}	max.	± 40	± 15	± 40	± 15	V
Gate-source voltage	V_{GS}	max.	± 40	$+15$ -30	± 40	$+15$ -40	V
Gate-drain voltage	V_{GD}	max.	± 40	$+15$ -30	± 40	$+15$ -40	V
Drain current (d.c.)	I_D	max.	50				mA
Total power dissipation up to $T_{amb} = 25^\circ\text{C}$ (free air)	P_{tot}	max.	275				mW
Storage temperature range	T_{stg}		-65 to $+175$				$^\circ\text{C}$
Junction temperature	T_j	max.	125				$^\circ\text{C}$

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	360	K/W
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CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

			BSD212	BSD213	BSD214	BSD215	
Drain-source breakdown voltage							
$V_{GS} = V_{BS} = -5\text{ V}; I_S = 10\text{ nA}$	$V_{(BR)DSX} >$		10	10	20	20	V
Source-drain breakdown voltage							
$V_{GD} = V_{BD} = -5\text{ V}; I_D = 10\text{ nA}$	$V_{(BR)SDX} >$		10	10	20	20	V
Drain-substrate breakdown voltage							
$V_{GB} = 0; I_D = 10\text{ nA};$ open source	$V_{(BR)DBO} >$		15	15	25	25	V
Source-substrate breakdown voltage							
$V_{GB} = 0; I_S = 10\text{ nA};$ open drain	$V_{(BR)SBO} >$		15	15	25	25	V
Drain-source leakage current							
$V_{GS} = V_{BS} = -5\text{ V}; V_{DS} = 10\text{ V}$	I_{DSoff}	typ.	1,0	1,0	—	—	nA
$V_{GS} = V_{BS} = -5\text{ V}; V_{DS} = 20\text{ V}$	I_{DSoff}	typ.	—	—	1,0	1,0	nA
Source-drain leakage current							
$V_{GD} = V_{BD} = -5\text{ V}; V_{SD} = 10\text{ V}$	I_{SDoff}	typ.	1,0	1,0	—	—	nA
$V_{GD} = V_{BD} = -5\text{ V}; V_{SD} = 20\text{ V}$	I_{SDoff}	typ.	—	—	1,0	1,0	nA
Gate-substrate leakage current							
$V_{DB} = V_{SB} = 0; V_{GB} = \pm 40\text{ V}$	I_{GBS}	$<$	0,1	—	0,1	—	nA
$V_{DB} = V_{SB} = 0; V_{GB} = \pm 15\text{ V}$	I_{GBS}	$<$	—	10	—	10	nA
Threshold voltage							
$V_{DS} = V_{GS} = V_{GS(th)}$ $V_{SB} = 0; I_S = 1\text{ }\mu\text{A}$	$V_{GS(th)}$		0,1 to 2,0				V

			BSD212	BSD213	BSD214	BSD215	
Drain-source resistance							
$I_D = 1,0\text{ mA}; V_{SB} = 0;$ $V_{GS} = 5\text{ V}$	$R_{DS(on)}$	typ.	50	50	50	50	Ω
		$<$	70	70	70	70	Ω
$V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ.	30	30	30	30	Ω
		$<$	45	45	45	45	Ω
$V_{GS} = 15\text{ V}$	$R_{DS(on)}$	typ.	25	25	25	25	Ω
$V_{GS} = 25\text{ V}$	$R_{DS(on)}$	typ.	15		15		Ω

DYNAMIC CHARACTERISTICS

Forward transconductance at $f = 1\text{ kHz}$							
$V_{DS} = 10\text{ V}; V_{SB} = 0; I_D = 20\text{ mA}$	g_{fs}	typ.		15			mS
		$>$		10			
Capacitance at $f = 1\text{ MHz}$ (see Fig. 2)							
$V_{GS} = V_{BS} = -15\text{ V}; V_{DS} = 10\text{ V}$							
Feed-back capacitance	C_{rss}	typ.		0,6			pF
Input capacitance	C_{iss}	typ.		2,3			pF
Output capacitance	C_{oss}	typ.		1,9			pF

DYNAMIC CHARACTERISTICS (continued)

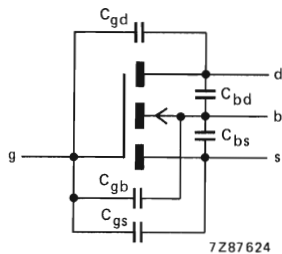


Fig. 2 Capacitances model.

$$C_{iss} = C_{GS} + C_{GD} + C_{GB}$$

$$C_{oss} = C_{GD} + C_{BD}$$

$$C_{rss} = C_{GD}$$

Switching times (see Fig. 3)

$V_{DD} = 10\text{ V}$; $V_i = -5\text{ V to } +5\text{ V}$

t_{on}	typ.	1,0	ns
t_{off}	typ.	5,0	ns

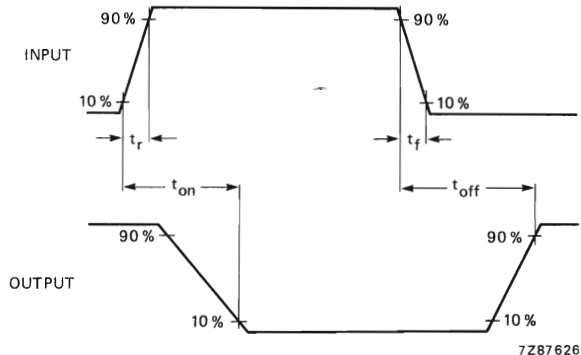
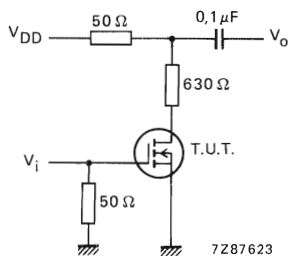


Fig. 3 Switching times test circuit and input and output waveforms.

Pulse generator:

$$R_i = 50\ \Omega$$

$$t_r < 0,5\text{ ns}$$

$$t_f < 1,0\text{ ns}$$

$$t_p = 20\text{ ns}$$

$$\delta < 0,01$$

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

The transistor is sealed in a SOT-143 envelope and features a low ON resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver

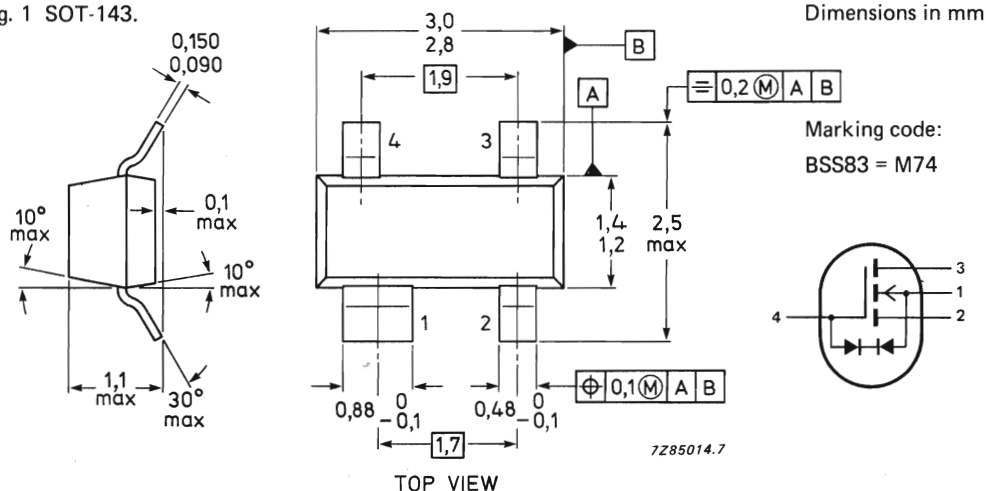
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	10 V
Source-drain voltage	V_{SD}	max.	10 V
Drain-substrate voltage	V_{DB}	max.	15 V
Source-substrate voltage	V_{SB}	max.	15 V
Drain current (d.c.)	I_D	max.	50 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	230 mW
Gate-source cut-off voltage			
$V_{DS} = V_{GS}; V_{SB} = 0;$	$V_{(P)GS}$	$>$	0,1 V
$I_D = 1\text{ }\mu\text{A}$		$<$	2,0 V
Drain-source ON-resistance			
$V_{GS} = 10\text{ V}; V_{SB} = 0; I_D = 0,1\text{ mA}$	$R_{DS(on)}$	$<$	45 Ω
Feed-back capacitance			
$V_{GS} = V_{BS} = -15\text{ V};$	C_{rss}	typ.	0,6 pF
$V_{DS} = 10\text{ V}; f = 1\text{ MHz}$			

MECHANICAL DATA

SOT-143 (see Fig. 1).

Fig. 1 SOT-143.



→ Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	10 V
Source-drain voltage	V_{SD}	max.	10 V
Drain-substrate voltage	V_{DB}	max.	15 V
Source-substrate voltage	V_{SB}	max.	15 V
Drain current (d.c.)	I_D	max.	50 mA
Total power dissipation up to $T_{amb} = 25\text{ °C}^*$	P_{tot}	max.	230 mW*
Storage temperature range	T_{stg}		-65 to +150 °C
Junction temperature	T_j	max.	125 °C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j-a}$	=	430 K/W*
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CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ unless otherwise specified

Drain-source breakdown voltage

$$V_{GS} = V_{BS} = -5\text{ V}; I_D = 10\text{ nA}$$

$$V_{(BR)DSX} > 10\text{ V}$$

Source-drain breakdown voltage

$$V_{GD} = V_{BD} = -5\text{ V}; I_D = 10\text{ nA}$$

$$V_{(BR)SDX} > 10\text{ V}$$

Drain-substrate breakdown voltage

$$V_{GB} = 0; I_D = 10\text{ nA}; \text{open source}$$

$$V_{(BR)DBO} > 15\text{ V}$$

Source-substrate breakdown voltage

$$V_{GB} = 0; I_D = 10\text{ nA}; \text{open drain}$$

$$V_{(BR)SBO} > 15\text{ V}$$

Drain-source leakage current

$$V_{GS} = V_{BS} = -2\text{ V}; V_{DS} = 6,6\text{ V}$$

$$I_{DSoff} < 10\text{ nA}$$

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Source-drain leakage current

$$V_{GD} = V_{BD} = -2 \text{ V}; V_{SD} = 6,6 \text{ V}$$

$$I_{SDoff} < 10 \text{ nA} \quad \leftarrow$$

Forward transconductance at $f = 1 \text{ kHz}$

$$V_{DS} = 10 \text{ V}; V_{SB} = 0; I_D = 20 \text{ mA}$$

$$g_{fs} > 10 \text{ mS}$$

$$\text{typ. } 15 \text{ mS}$$

Gate-source cut-off voltage

$$V_{DS} = V_{GS}; V_{SB} = 0; I_D = 1 \mu\text{A}$$

$$V_{(P)GS} > 0,1 \text{ V}$$

$$< 2,0 \text{ V}$$

Drain-source ON-resistance

$$I_D = 0,1 \text{ mA};$$

$$V_{GS} = 5 \text{ V}; V_{SB} = 0$$

$$V_{GS} = 10 \text{ V}; V_{SB} = 0$$

$$V_{GS} = 3,2 \text{ V}; V_{SB} = 6,8 \text{ V (see Fig. 4)}$$

$$R_{DS(on)} < 70 \Omega$$

$$R_{DS(on)} < 45 \Omega$$

$$R_{DS(on)} \text{ typ. } 80 \Omega$$

$$< 120 \Omega$$

Gate-substrate zener voltages

$$V_{DB} = V_{SB} = 0; -I_C = 10 \mu\text{A}$$

$$V_{Z(1)} > 12,5 \text{ V}$$

$$V_{DB} = V_{SB} = 0; +I_G = 10 \mu\text{A}$$

$$V_{Z(2)} > 12,5 \text{ V}$$

Capacitances at $f = 1 \text{ MHz}$

$$V_{GS} = V_{BS} = -15 \text{ V}; V_{DS} = 10 \text{ V}$$

Feed-back capacitance

$$C_{rss} \text{ typ. } 0,6 \text{ pF}$$

Input capacitance

$$C_{iss} \text{ typ. } 1,5 \text{ pF}$$

Output capacitance

$$C_{oss} \text{ typ. } 1,0 \text{ pF}$$

Switching times (see Fig. 2)

$$V_{DD} = 10 \text{ V}; V_i = 5 \text{ V}$$

$$t_{on} \text{ typ. } 1,0 \text{ ns}$$

$$t_{off} \text{ typ. } 5,0 \text{ ns}$$

Pulse generator:

$$R_i = 50 \Omega$$

$$t_r < 0,5 \text{ ns}$$

$$t_f < 1,0 \text{ ns}$$

$$t_p = 20 \text{ ns}$$

$$\delta < 0,01$$

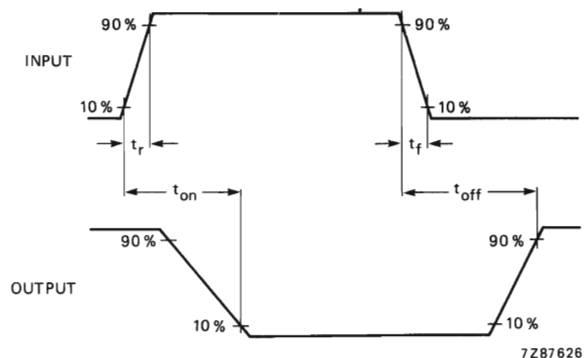
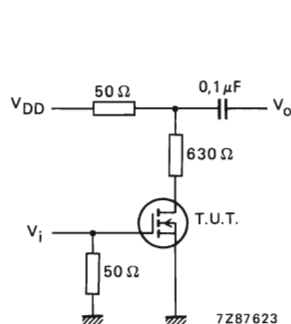
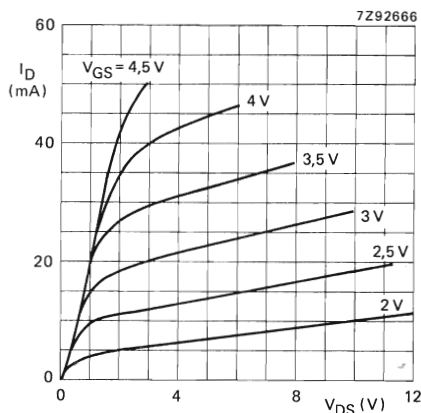
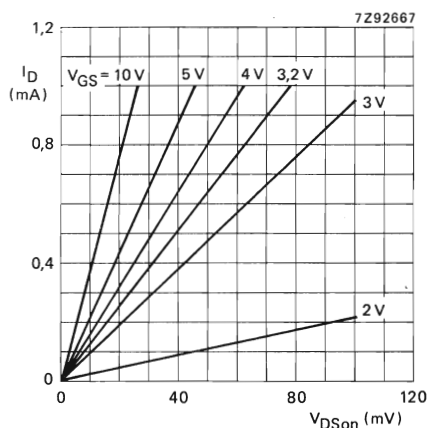
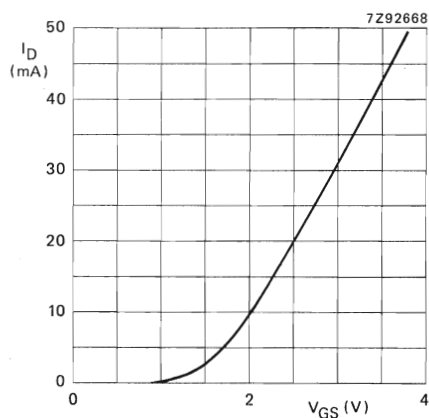
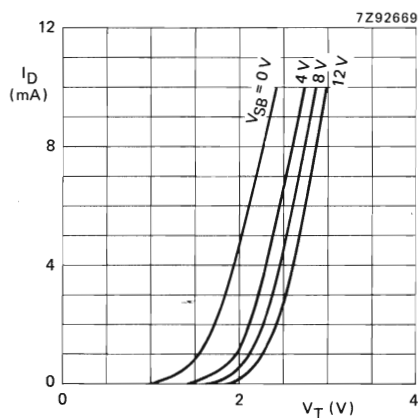
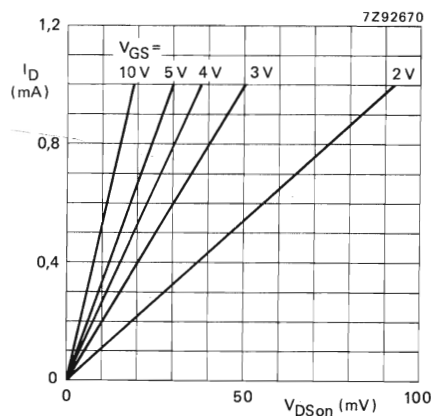


Fig. 2 Switching times test circuit and input and output waveforms.

Fig. 3 $V_{SB} = 0$; typical values.Fig. 4 $V_{SB} = 6.8$ V; typical values.Fig. 5 $V_{DS} = 10$ V; $V_{SB} = 0$; typical values.Fig. 6 $V_{DS} = V_{GS} = V_T$.Fig. 7 $V_{SB} = 0$; typical values.

Conditions for Figs 3, 4, 5, 6 and 7:
 $T_j = 25$ °C.

N-CHANNEL IG-MOS-FET

Symmetrical depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for chopper and other special switching applications, e.g. timing circuits, multiplex circuits, etc. The features are a very low drain-source 'on' resistance, a very high drain-source 'off' resistance and low feedback capacitances.

QUICK REFERENCE DATA

Drain-source resistance (on) at $f = 1 \text{ kHz}$

$$V_{DS} = 0; V_{GS} = 5 \text{ V}; V_{BS} = 0$$

$$r_{ds \text{ on}} < 50 \text{ } \Omega$$

Drain-source resistance (off)

$$V_{DS} = 10 \text{ V}; -V_{GS} = 5 \text{ V}; V_{BS} = 0$$

$$r_{DSoff} > 10 \text{ G}\Omega$$

Feedback capacitance at $f = 1 \text{ MHz}$

$$-V_{GS} = 5 \text{ V}; V_{DS} = 0; I_B = 0$$

$$C_{rs} < 0,5 \text{ pF}$$

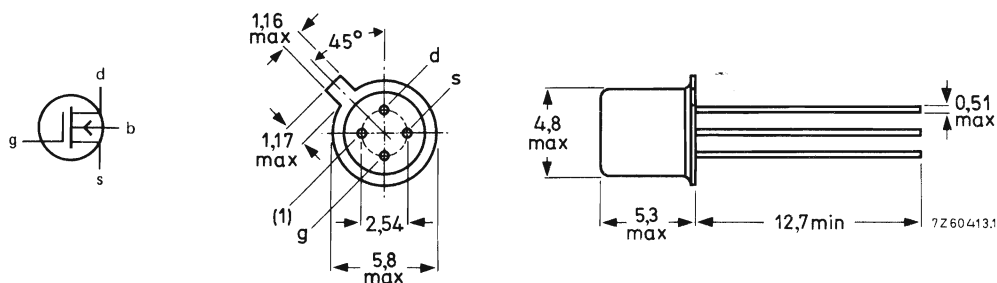
$$-V_{GD} = 5 \text{ V}; V_{SD} = 0; I_B = 0$$

$$C_{rd} < 0,5 \text{ pF}$$

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = substrate connected to case.

Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-substrate voltage	V_{DB}	max.	30 V
Source-substrate voltage	V_{SB}	max.	30 V
Gate-substrate voltage (continuous)	V_{GB}	max.	10 V
		min.	-10 V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	V_{G-N}	max.	15 V
		min.	-15 V
Non-repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $t < 10$ ms	V_{G-N}	max.	50 V
		min.	-50 V
→ Drain current (d.c.)	I_D	max.	25 mA
Drain current (peak value) $t_r = 20$ ms; $\delta = 0,1$	I_{DM}	max.	50 mA
Source current (peak value) $t_r = 20$ ms; $\delta = 0,1$	I_{SM}	max.	50 mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	200 mW
Storage temperature	T_{stg}	-65 to + 125 °C	
Junction temperature	T_j	max.	125 °C

THERMAL RESISTANCE

From junction to ambient in free air	R_{thj-a}	=	0,5 °C/mW
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CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Drain cut-off currents; $V_{BS} = 0$

$V_{DS} = 10\text{ V}$; $-V_{GS} = 5\text{ V}$ $I_{DSX} < 1\text{ nA}$

$V_{DS} = 10\text{ V}$; $-V_{GS} = 5\text{ V}$; $T_j = 125\text{ }^{\circ}\text{C}$ $I_{DSX} < 1\text{ }\mu\text{A}$

Source cut-off currents; $V_{BD} = 0$

$V_{SD} = 10\text{ V}$; $-V_{GD} = 5\text{ V}$ $I_{SDX} < 1\text{ nA}$

$V_{SD} = 10\text{ V}$; $-V_{GD} = 5\text{ V}$; $T_j = 125\text{ }^{\circ}\text{C}$ $I_{SDX} < 1\text{ }\mu\text{A}$

Gate currents; $V_{BS} = 0$

$-V_{GS} = 10\text{ V}$; $V_{DS} = 0$ $-I_{GSS} < 10\text{ pA}$

$V_{GS} = 10\text{ V}$; $V_{DS} = 0$ $I_{GSS} < 10\text{ pA}$

$-V_{GS} = 10\text{ V}$; $V_{DS} = 0$; $T_j = 125\text{ }^{\circ}\text{C}$ $-I_{GSS} < 200\text{ pA}$

$V_{GS} = 10\text{ V}$; $V_{DS} = 0$; $T_j = 125\text{ }^{\circ}\text{C}$ $I_{GSS} < 200\text{ pA}$

Bulk currents; $V_{GB} = 0$

$-V_{BD} = 30\text{ V}$; $I_S = 0$ $-I_{BDO} < 10\text{ }\mu\text{A}$

$-V_{BS} = 30\text{ V}$; $I_D = 0$ $-I_{BSO} < 10\text{ }\mu\text{A}$

Drain-source resistance (on) at $f = 1\text{ kHz}$; $V_{BS} = 0$

$V_{GS} = 0$; $V_{DS} = 0$ $r_{dson} < 100\text{ }\Omega$

$V_{GS} = 0$; $V_{DS} = 0$; $T_j = 125\text{ }^{\circ}\text{C}$ $r_{dson} < 150\text{ }\Omega$

$+V_{GS} = 5\text{ V}$; $V_{DS} = 0$ $r_{dson} < 50\text{ }\Omega$

Drain-source resistance (off)

$-V_{GS} = 5\text{ V}$; $V_{DS} = 10\text{ V}$; $V_{BS} = 0$ $r_{DSoff} > 10\text{ G}\Omega$

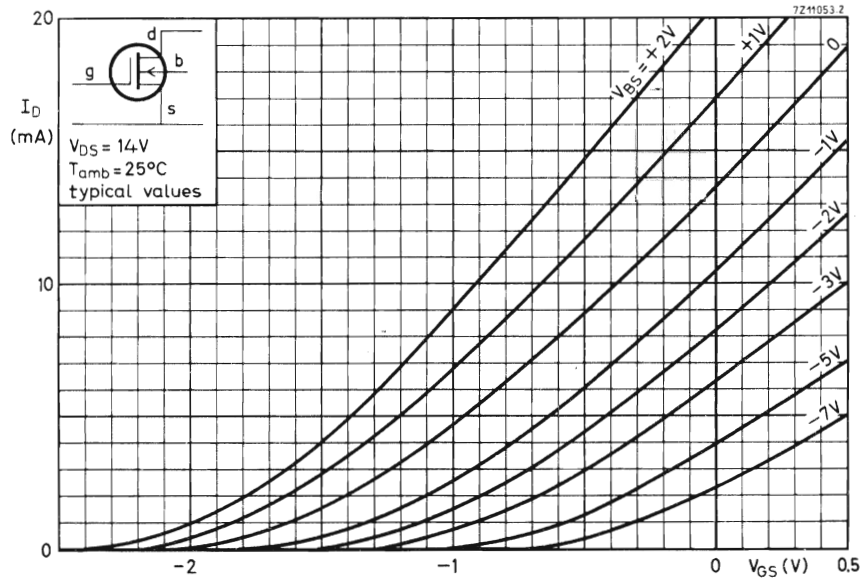
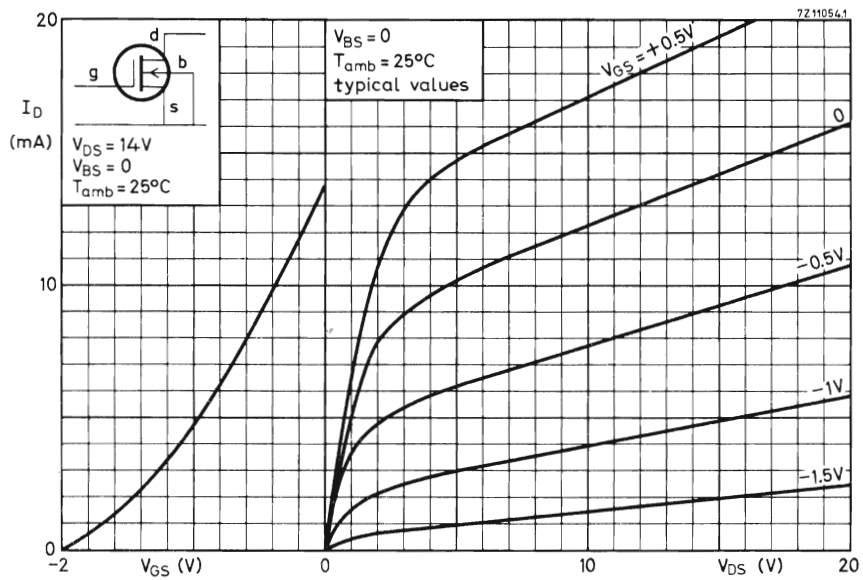
Feedback capacitances at $f = 1\text{ MHz}$

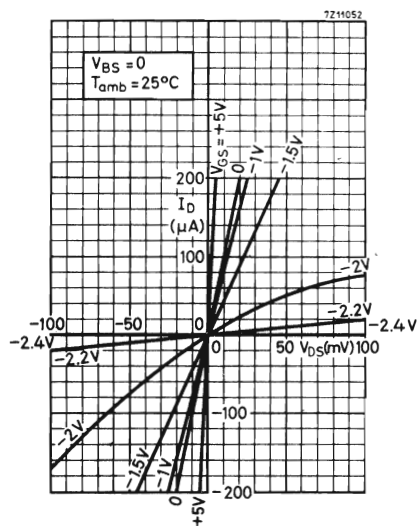
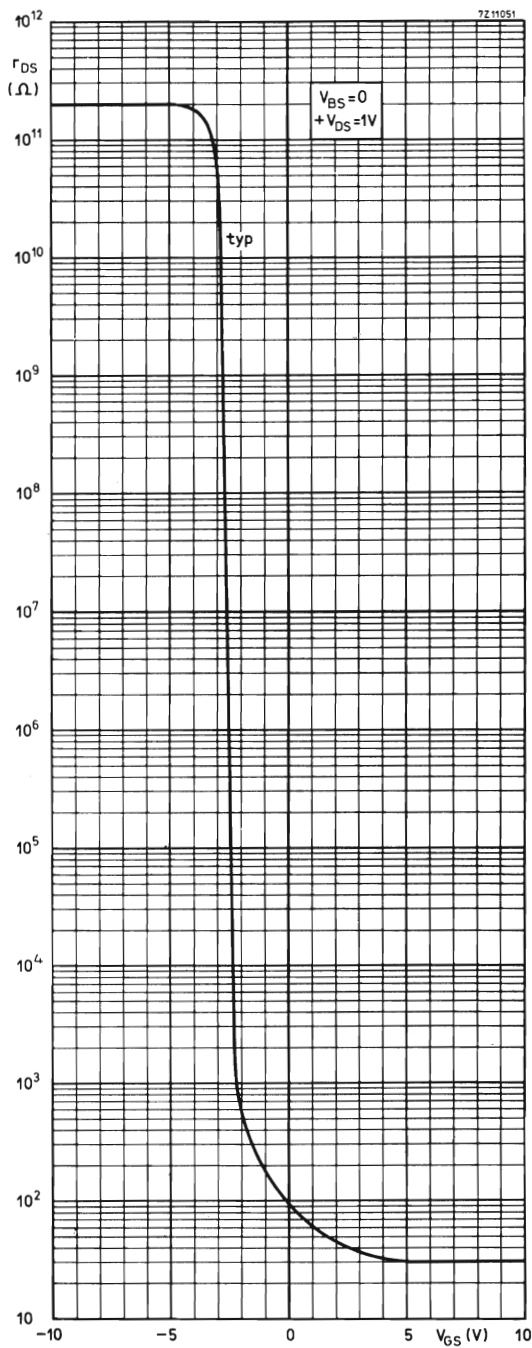
$-V_{GS} = 5\text{ V}$; $V_{DS} = 0$; $I_B = 0$ $C_{rs} < 0,5\text{ pF}$

$-V_{GD} = 5\text{ V}$; $V_{SD} = 0$; $I_B = 0$ $C_{rd} < 0,5\text{ pF}$

Gate to all other terminals capacitance at $f = 1\text{ MHz}$

$-V_{GB} = 5\text{ V}$; $V_{SB} = V_{DB} = 0$ $C_{g-n} < 6\text{ pF}$





DEVICE DATA

MOS-FETS

dual gate

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for use in u.h.f. applications in television tuners and professional communication equipment.

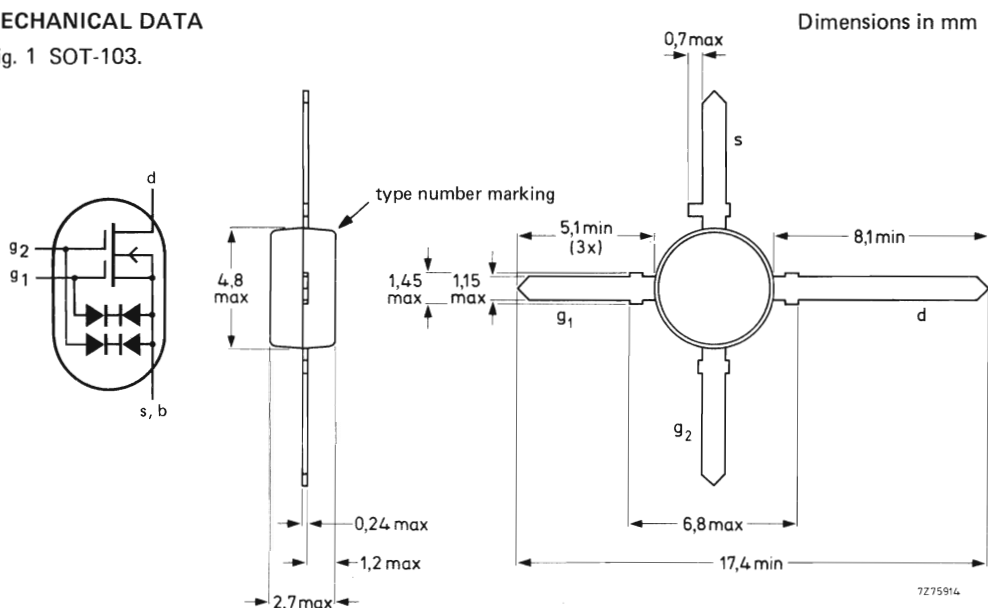
This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current (peak value)	I_{DM}	max.	30 mA
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 7\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	12 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 7\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25 fF
Noise figure at $G_S = 2\text{ mS}$; $B_S = B_S\text{ opt}$ $I_D = 7\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 800\text{ MHz}$	F	typ.	2,8 dB
Power gain at $f = 800\text{ MHz}$ $I_D = 7\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $G_S = 2\text{ mS}$; $B_S = B_S\text{ opt}$; $G_L = 1\text{ mS}$; $B_L = B_L\text{ opt}$	G_p	typ.	16,5 dB

MECHANICAL DATA

Fig. 1 SOT-103.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

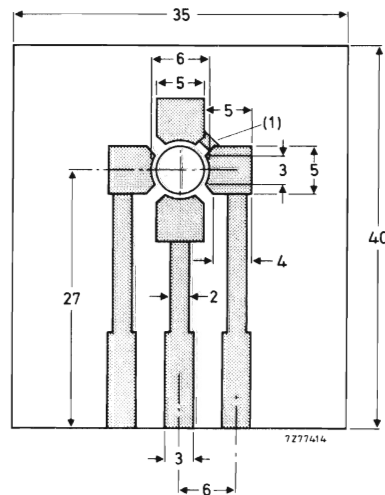
Drain-source voltage	V_{DS}	max.	20 V
Drain current (d.c. or average)	I_D	max.	20 mA
Drain current (peak value)	I_{DM}	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	225 mW
Storage temperature	T_{stg}	max.	-65 to $+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	$150\text{ }^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air
mounted on the printed-circuit board

$$R_{th\ j-a} = 335\text{ K/W}$$

Dimensions in mm



(1) Connection made by
a strip or Cu wire.

Fig. 2 Single-sided $35\text{ }\mu\text{m}$ Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS $T_{amb} = 25\text{ }^{\circ}\text{C}$

Gate cut-off currents

 $\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$ $\pm I_{G1-SS} < 50\text{ nA}$ $\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$ $\pm I_{G2-SS} < 50\text{ nA}$

Gate-source breakdown voltages

 $\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$ $\pm V_{(BR)G1-SS} 6,0\text{ to }20\text{ V}$ $\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$ $\pm V_{(BR)G2-SS} 6,0\text{ to }20\text{ V}$

Drain current*

 $V_{DS} = 10\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}$ $I_{DSS} 2\text{ to }20\text{ mA}$

Gate-source cut-off voltages

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$ $-V_{(P)G1-S} < 2,7\text{ V}$ $I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$ $-V_{(P)G2-S} < 2,7\text{ V}$ **DYNAMIC CHARACTERISTICS**Measuring conditions (common source): $I_D = 7\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at $f = 1\text{ kHz}$ $|Y_{fs}| > 9,5\text{ mS}$
typ. 12 mSInput capacitance at gate 1; $f = 1\text{ MHz}$ C_{ig1-s} typ. 1,8 pFInput capacitance at gate 2; $f = 1\text{ MHz}$ C_{ig2-s} typ. 1,0 pFFeedback capacitance at $f = 1\text{ MHz}$ C_{rs} typ. 25 fFOutput capacitance at $f = 1\text{ MHz}$ C_{os} typ. 0,9 pFNoise figure at $G_S = 2\text{ mS}; B_S = B_S\text{ opt}$ $f = 200\text{ MHz}$ F typ. 1,6 dB ← $f = 800\text{ MHz}$ F typ. 2,8 dBPower gain at $G_S = 2\text{ mS}; B_S = B_S\text{ opt}$ $G_L = 0,5\text{ mS}; B_L = B_L\text{ opt}; f = 200\text{ MHz}$ G_p typ. 23 dB ← $G_L = 1\text{ mS}; B_L = B_L\text{ opt}; f = 800\text{ MHz}$ G_p typ. 16,5 dB ←

* Measured under pulse conditions.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications in television tuners, especially in r.f. stages and mixer stages in S-channel tuners. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

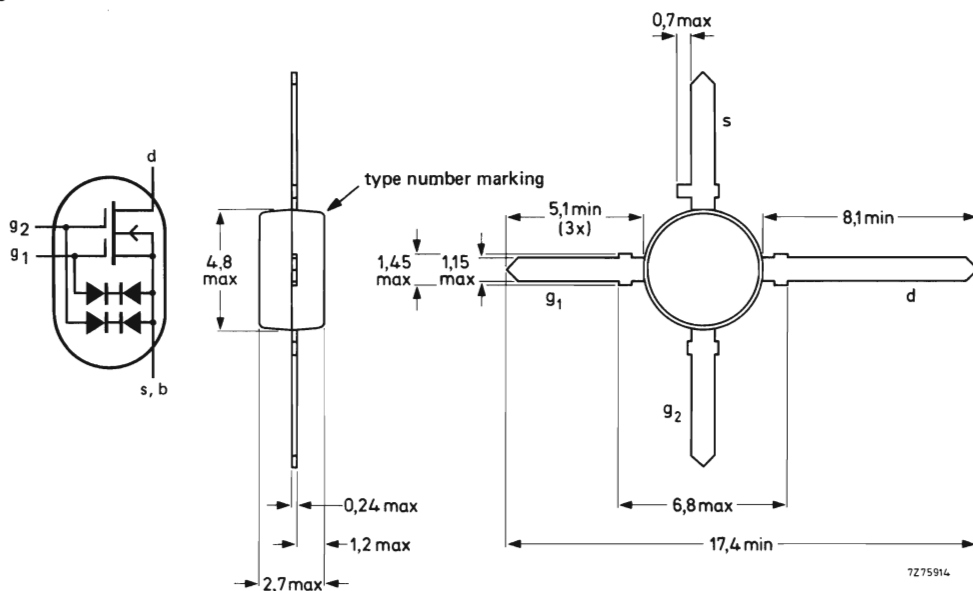
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain-current	I_D	max.	30 mA
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	17 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$, $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25 fF
Noise figure at $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 200\text{ MHz}$	F	typ.	1,5 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain-current (d.c. or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	225 mW
Storage temperature	T_{stg}	-65 to +150	$^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

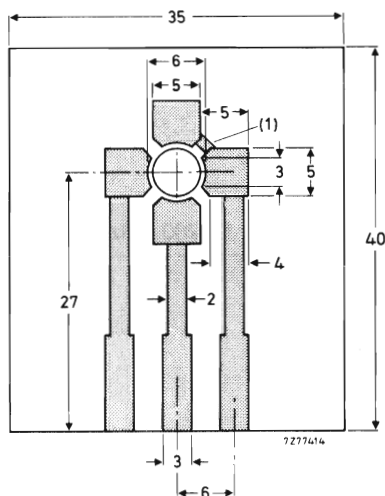
THERMAL RESISTANCE

From junction to ambient in free air

mounted on the printed-circuit board (see Fig. 2)

$$R_{th\ j-a} = 335\text{ K/W}$$

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$

Gate cut-off currents

$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$

$\pm I_{G1-SS} < 50\text{ nA}$

$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$

$\pm I_{G2-SS} < 50\text{ nA}$

Gate-source breakdown voltages

$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$

$\pm V_{(BR)G1-SS} \quad 6,0\text{ to }20\text{ V}$

$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$

$\pm V_{(BR)G2-SS} \quad 6,0\text{ to }20\text{ V}$

Drain current*

$V_{DS} = 15\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}$

$I_{DSS} \quad 2\text{ to }20\text{ mA}$

Gate-source cut-off voltages

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$

$-V_{(P)G1-S} < 2,5\text{ V}$

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; V_{G1-S} = 0$

$-V_{(P)G2-S} < 2,0\text{ V}$

DYNAMIC CHARACTERISTICS

Measuring conditions (common source); $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at $f = 1\text{ kHz}$

$|y_{fs}| \begin{matrix} > 15\text{ mS} \\ \text{typ.} & 17\text{ mS} \end{matrix}$

Input capacitance at gate 1; $f = 1\text{ MHz}$

$C_{ig1-s} \begin{matrix} \text{typ.} & 2,5\text{ pF} \\ < & 3,0\text{ pF} \end{matrix}$

Input capacitance at gate 2; $f = 1\text{ MHz}$

$C_{ig2-s} \quad \text{typ.} \quad 1,2\text{ pF}$

Feedback capacitance at $f = 1\text{ MHz}$

$C_{rs} \begin{matrix} \text{typ.} & 25\text{ fF} \\ < & 35\text{ fF} \end{matrix}$

Output capacitance at $f = 1\text{ MHz}$

$C_{os} \begin{matrix} \text{typ.} & 1,0\text{ pF} \\ < & 1,3\text{ pF} \end{matrix}$

Noise figure at $G_S = 2\text{ mS}; B_S = B_S\text{ opt}$
 $f = 200\text{ MHz}$

$F \begin{matrix} \text{typ.} & 1,5\text{ dB} \\ < & 2,8\text{ dB} \end{matrix}$

Power gain at $G_S = 2\text{ mS}; B_S = B_S\text{ opt}$
 $G_L = 0,5\text{ mS}; B_L = B_L\text{ opt}; f = 200\text{ MHz}$

$G_p \quad \text{typ.} \quad 25\text{ dB}$

* Measured under pulse conditions.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications in television tuners. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

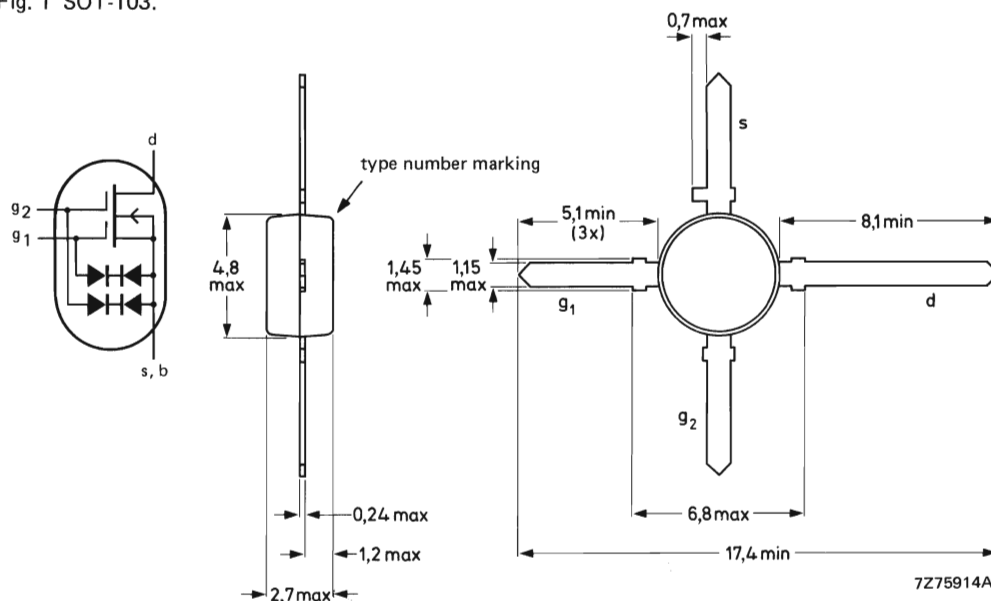
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain-current	I_D	max.	50 mA
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	18 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25 fF
Noise figure at $G_S = 2\text{ mS}$; $B_S = B_S\text{ opt}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 200\text{ MHz}$	F	typ.	1,0 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain-current (d.c. or average)	I_D	max.	50 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	225 mW
Storage temperature	T_{stg}		$-65\text{ to }+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

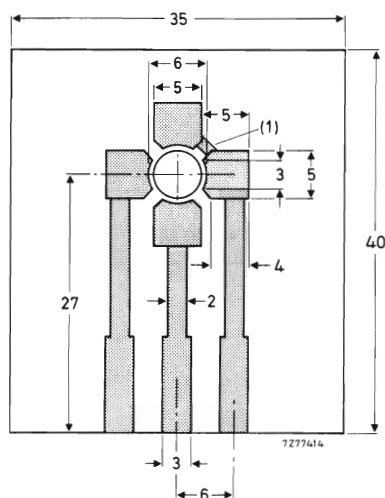
THERMAL RESISTANCE

From junction to ambient in free air

mounted on the printed-circuit board (see Fig. 2)

$$R_{th\ j-a} = 335\text{ K/W}$$

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$

Gate cut-off currents

 $\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$ $\pm I_{G1-SS} < 50\text{ nA}$ $\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$ $\pm I_{G2-SS} < 50\text{ nA}$

Gate-source breakdown voltages

 $\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$ $\pm V_{(BR)G1-SS} 6,0\text{ to }20\text{ V}$ $\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$ $\pm V_{(BR)G2-SS} 6,0\text{ to }20\text{ V}$

Drain current (measured under pulse conditions)

 $V_{DS} = 15\text{ V}; V_{G1-S} = 0; + V_{G2-S} = 4\text{ V}$ $I_{DSS} 4\text{ to }20\text{ mA}$

Gate-source cut-off voltages

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; + V_{G2-S} = 4\text{ V}$ $-V_{(P)G1-S} < 2,5\text{ V}$ $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; V_{G1-S} = 0$ $-V_{(P)G2-S} < 2,0\text{ V}$

DYNAMIC CHARACTERISTICS

Measuring conditions (common source); $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; + V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at $f = 1\text{ kHz}$ $|y_{fs}| > 15\text{ mS}$
typ. 18 mSInput capacitance at gate 1; $f = 1\text{ MHz}$ C_{ig1-s} typ. 2,5 pF
< 3,0 pFInput capacitance at gate 2; $f = 1\text{ MHz}$ C_{ig2-s} typ. 1,2 pFFeedback capacitance at $f = 1\text{ MHz}$ C_{rs} typ. 25 fF ←Output capacitance at $f = 1\text{ MHz}$ C_{os} typ. 1,0 pF ←Noise figure at $G_S = 2\text{ mS}; B_S = B_S\text{ opt}$
 $f = 200\text{ MHz}$ F typ. 1,0 dB ←Power gain at $G_S = 2\text{ mS}; B_S = B_S\text{ opt}$
 $G_L = 0,5\text{ mS}; B_L = B_L\text{ opt}; f = 200\text{ MHz}$ G_p typ. 25 dB ←

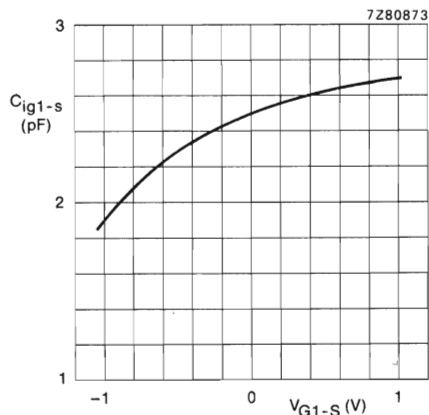


Fig. 3 $V_{G2-S} = 4 \text{ V}$; $V_{DS} = 15 \text{ V}$;
 $f = 1 \text{ MHz}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; typical values.

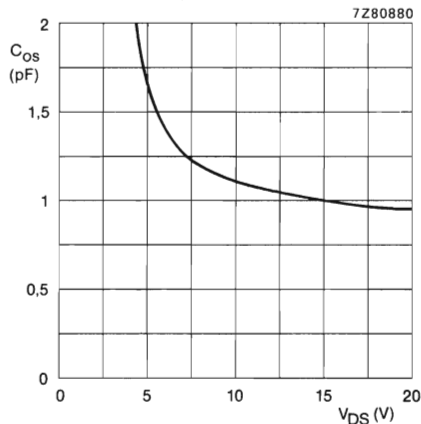


Fig. 5 $V_{G2-S} = 4 \text{ V}$; $I_D = 10 \text{ mA}$;
 $f = 1 \text{ MHz}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; typical values.

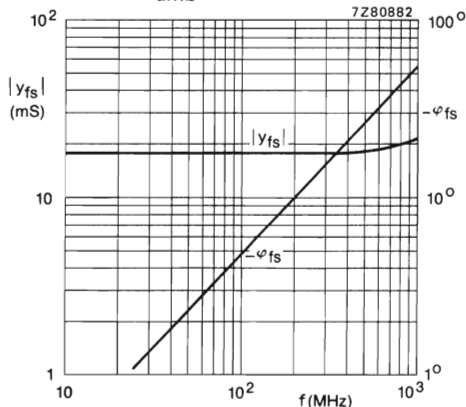


Fig. 7 $V_{G2-S} = 4 \text{ V}$; $V_{GS} = 15 \text{ V}$;
 $I_D = 10 \text{ mA}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; typical values.

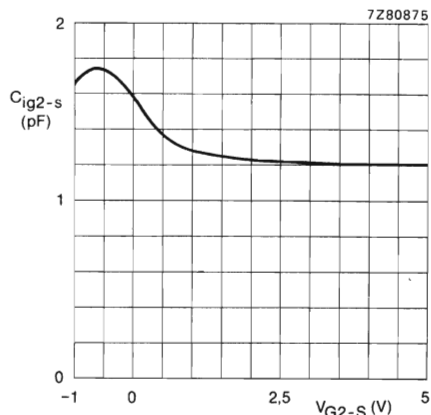


Fig. 4 $V_{G1-S} = 0 \text{ V}$; $V_{DS} = 15 \text{ V}$;
 $f = 1 \text{ MHz}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; typical values.

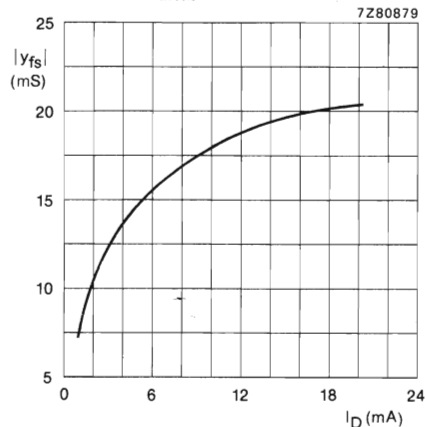


Fig. 6 $V_{G2-S} = 4 \text{ V}$; $V_{DS} = 15 \text{ V}$;
 $f = 1 \text{ kHz}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; typical values.

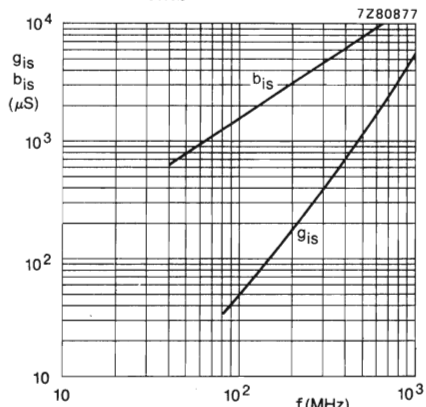


Fig. 8 $V_{G2-S} = 4 \text{ V}$; $V_{DS} = 15 \text{ V}$;
 $I_D = 10 \text{ mA}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; typical values.

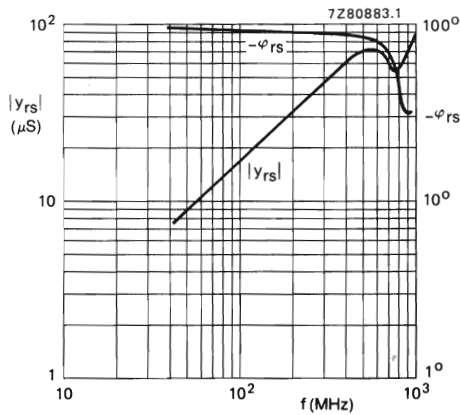


Fig. 9 $V_{G2-S} = 4 \text{ V}$; $V_{DS} = 15 \text{ V}$;
 $I_D = 10 \text{ mA}$; $T_{amb} = 25^\circ\text{C}$; typical values.

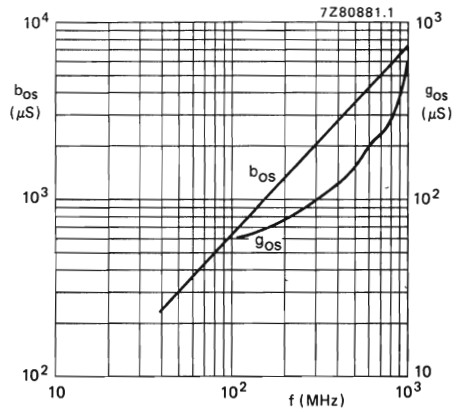


Fig. 10 $V_{G2-S} = 4 \text{ V}$; $V_{DS} = 15 \text{ V}$;
 $I_D = 10 \text{ mA}$; $T_{amb} = 25^\circ\text{C}$; typical values.

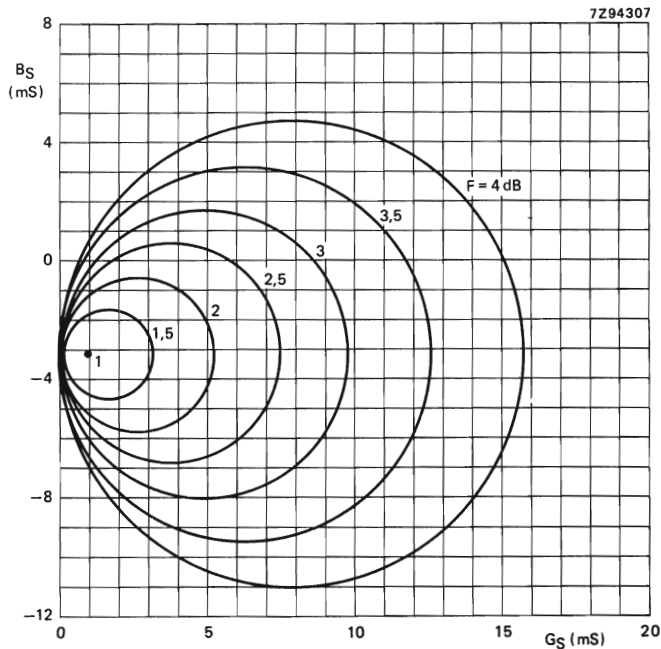


Fig. 11 $V_{G2-S} = 4 \text{ V}$; $V_{DS} = 15 \text{ V}$; $I_D = 10 \text{ mA}$; $f = 200 \text{ MHz}$; $T_{amb} = 25^\circ\text{C}$; typical values.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in plastic X-package with source and substrate interconnected, intended for v.h.f. applications, such as v.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

This device is especially intended for use in pre-amplifiers in CATV tuners with large tuning ranges up to 500 MHz.

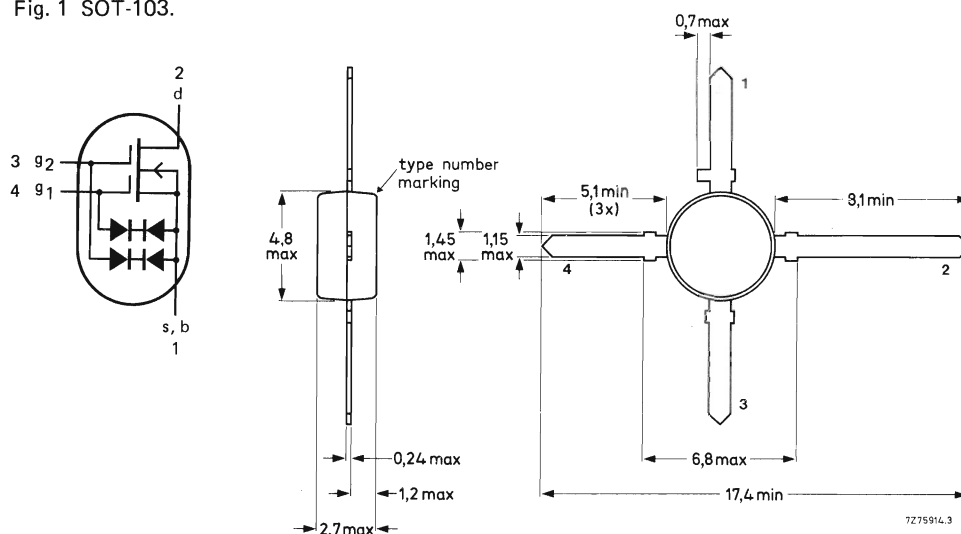
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain-current	I_D	max.	30 mA
Total power dissipation up to $T_{amb} = 75^\circ\text{C}$	P_{tot}	max.	225 mW
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	18 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25 fF
Noise figure at $G_S = 2\text{ mS}$; $B_S = B_{Sopt}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $V_{G2-S} = 4\text{ V}$; $f = 200\text{ MHz}$	F	typ.	1,0 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain-current (d.c. or average)	I_D	max.	30 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	225 mW
Storage temperature	T_{stg}	$-65\text{ to }+150\text{ }^{\circ}\text{C}$	
Junction temperature	T_j	max.	$150\text{ }^{\circ}\text{C}$

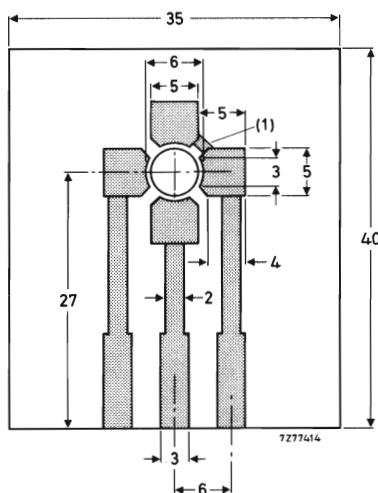
THERMAL RESISTANCE

From junction to ambient in free air

mounted on a printed-circuit board (see Fig. 2)

$$R_{th\ i-a} = 335\text{ K/W}$$

Dimensions in mm



(1) Connection made by a strip or Cu wire

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless stated otherwise

Gate cut-off currents

 $\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$ $\pm I_{G1-SS} < 50\text{ nA}$ $\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$ $\pm I_{G2-SS} < 50\text{ nA}$

Gate-source breakdown voltages

 $\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$ $\pm V_{(BR)G1-SS} 6,0\text{ to }20\text{ V}$ $\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$ $\pm V_{(BR)G2-SS} 6,0\text{ to }20\text{ V}$

Drain current

 $V_{DS} = 15\text{ V}; V_{G1-S} = 0;$ $V_{G2-S} = 4\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$ $I_{DSS} 2,0\text{ to }20\text{ mA}$

Gate-source cut-off voltages

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$ $-V_{(P)G1-S} < 2,5\text{ V}$ $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; +V_{G1-S} = 0$ $-V_{(P)G2-S} < 2,0\text{ V}$ **DYNAMIC CHARACTERISTICS**Measuring conditions (common source); $I_D = 10\text{ mA};$ $V_{DS} = 15\text{ V}; V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at $f = 1\text{ kHz}$ $|y_{fs}| > 15\text{ mS}$
typ. 18 mSInput capacitance at gate 1 at $f = 1\text{ MHz}$ C_{ig1-s} typ. 2,5 pFInput capacitance at gate 2 at $f = 1\text{ MHz}$ C_{ig2-s} typ. 1,2 pFFeedback capacitance at $f = 1\text{ MHz}$ C_{rs} typ. 25 fFOutput capacitance at $f = 1\text{ MHz}$ C_{os} typ. 1,0 pFNoise figure at $G_S = 2\text{ mS}; B_S = B_{Sopt}$
and $f = 200\text{ MHz}$ F typ. 1,0 dBPower gain at $G_S = 2\text{ mS}; B_S = B_{Sopt}$
 $G_L = 0,5\text{ mS}; B_L = B_{Lopt}; f = 200\text{ MHz}$ G_p typ. 25 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

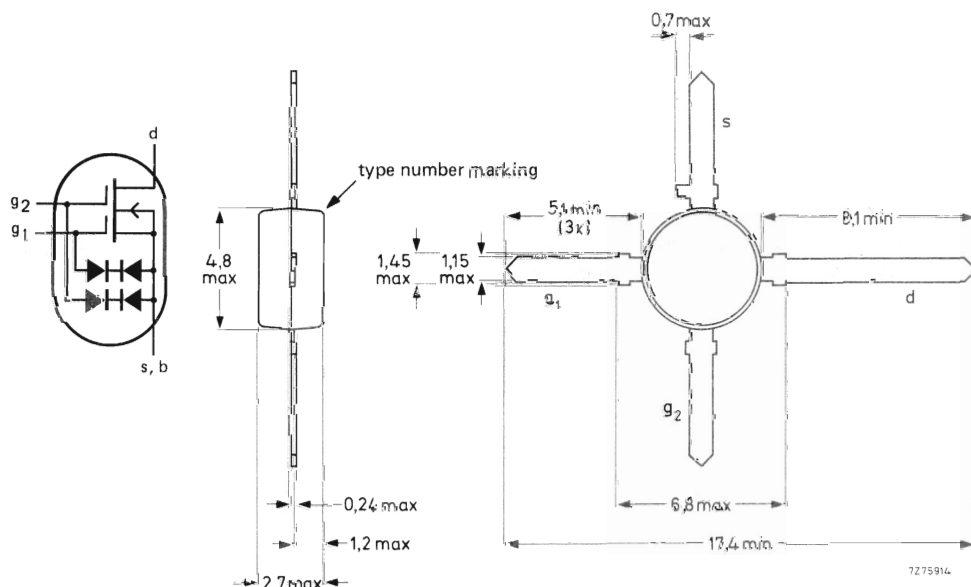
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain-current	I_D	max.	30 mA
Total power dissipation up to $T_{amb} = 75^\circ\text{C}$	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 $^\circ\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	17 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25 fF
Noise figure at $G_S = 2\text{ mS}$; $B_S = B_S\text{ opt}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 800\text{ MHz}$	F	typ.	2,8 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



STATIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$

Gate cut-off currents

$$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0 \quad \pm I_{G1-SS} < 50\text{ nA}$$

$$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0 \quad \pm I_{G2-SS} < 50\text{ nA}$$

Gate-source breakdown voltages

$$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0 \quad \pm V_{(BR)G1-SS} 6,0\text{ to }20\text{ V}$$

$$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0 \quad \pm V_{(BR)G2-SS} 6,0\text{ to }20\text{ V}$$

Drain current*

$$V_{DS} = 15\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V} \quad I_{DSS} 2\text{ to }20\text{ mA}$$

Gate-source cut-off voltages

$$I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V} \quad -V_{(P)G1-S} < 2,5\text{ V}$$

$$I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; V_{G1-S} = 0 \quad -V_{(P)G2-S} < 2,0\text{ V}$$

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at $f = 1\text{ kHz}$

$$|y_{fs}| > 15\text{ mS}$$

$$\text{typ. } 17\text{ mS}$$

Input capacitance at gate 1; $f = 1\text{ MHz}$

$$C_{ig1-s} \text{ typ. } 2,2\text{ pF}$$

$$< 2,6\text{ pF}$$

Input capacitance at gate 2; $f = 1\text{ MHz}$

$$C_{ig2-s} \text{ typ. } 1,1\text{ pF}$$

Feedback capacitance at $f = 1\text{ MHz}$

$$C_{rs} \text{ typ. } 25\text{ fF}$$

$$< 35\text{ fF}$$

Output capacitance at $f = 1\text{ MHz}$

$$C_{os} \text{ typ. } 0,8\text{ pF}$$

$$< 1,2\text{ pF}$$

Noise figure at $G_S = 2\text{ mS}; B_S = B_S \text{ opt}$
 $f = 200\text{ MHz}$

$$F \text{ typ. } 1,5\text{ dB}$$

 $f = 800\text{ MHz}$

$$F \text{ typ. } 2,8\text{ dB}$$

$$< 3,9\text{ dB}$$

Power gain at $G_S = 2\text{ mS}; B_S = B_S \text{ opt}$ $G_L = 0,5\text{ mS}; B_L = B_L \text{ opt}; f = 200\text{ MHz}$

$$G_p \text{ typ. } 25\text{ dB}$$

 $G_L = 1\text{ mS}; B_L = B_L \text{ opt}; f = 800\text{ MHz}$

$$G_p \text{ typ. } 18\text{ dB}$$

* Measured under pulse conditions.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

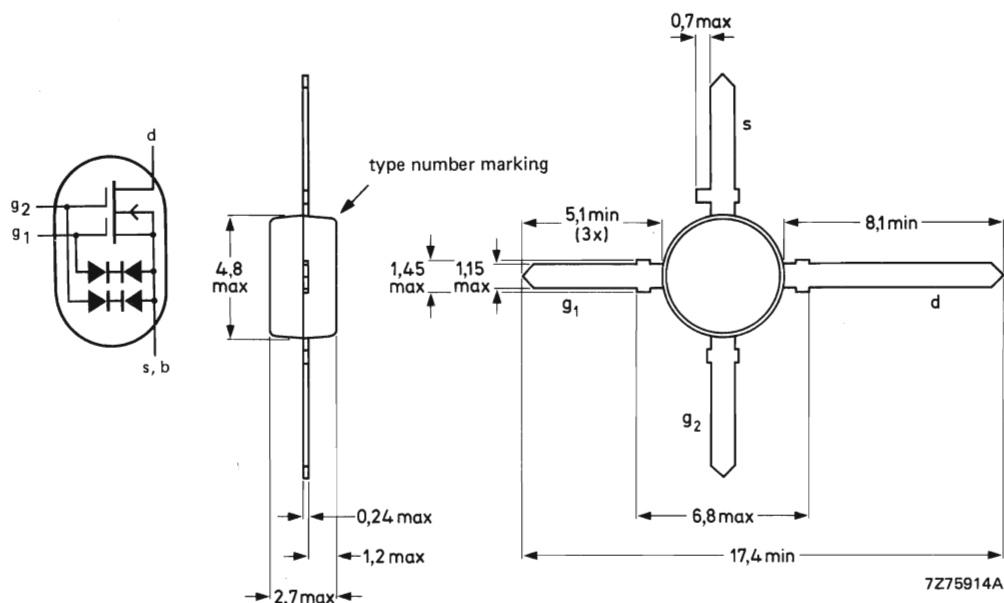
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain-current	I_D	max.	30 mA
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	18 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25 fF
Noise figure at $G_S = 3,3\text{ mS}$; $B_S = B_{S\text{ opt}}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 800\text{ MHz}$	F	typ.	1,8 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



STATIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$

Gate cut-off currents

$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$

$\pm I_{G1-SS} < 50\text{ nA}$

$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$

$\pm I_{G2-SS} < 50\text{ nA}$

Gate-source breakdown voltages

$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$

$\pm V_{(BR)G1-SS} \quad 6,0\text{ to }20\text{ V}$

$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$

$\pm V_{(BR)G2-SS} \quad 6,0\text{ to }20\text{ V}$

Drain current (measured under pulse conditions)

$V_{DS} = 15\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}$

$I_{DSS} \quad 4\text{ to }20\text{ mA}$

Gate-source cut-off voltages

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$

$-V_{(P)G1-S} < 2,5\text{ V}$

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; V_{G1-S} = 0$

$-V_{(P)G2-S} < 2,0\text{ V}$

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at $f = 1\text{ kHz}$

$|Y_{fs}| > 15\text{ mS}$
typ. 18 mS

Input capacitance at gate 1; $f = 1\text{ MHz}$

C_{ig1-s} typ. 2,3 pF
< 2,6 pF

Input capacitance at gate 2; $f = 1\text{ MHz}$

C_{ig2-s} typ. 1,1 pF

Feedback capacitance at $f = 1\text{ MHz}$

C_{rs} typ. 25 fF

Output capacitance at $f = 1\text{ MHz}$

C_{os} typ. 0,8 pF

Noise figure

$f = 200\text{ MHz}; G_S = 2\text{ mS}; B_S = B_S\text{ opt}$

F typ. 1,0 dB

$f = 800\text{ MHz}; G_S = 3,3\text{ mS}; B_S = B_S\text{ opt}$

F typ. 1,8 dB

Power gain

$f = 200\text{ MHz}; G_S = 2\text{ mS}; G_L = 0,5\text{ mS}; B_S = \text{opt}; B_L = \text{opt}$

G_p typ. 25 dB

$f = 800\text{ MHz}; G_S = 3,3\text{ mS}; G_L = 1\text{ mS}; B_S = \text{opt}; B_L = \text{opt}$

G_p typ. 18 dB

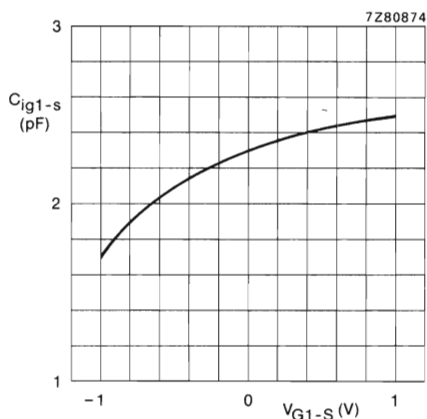


Fig. 3 $V_{G2-S} = 4\text{ V}; V_{DS} = 15\text{ V};$
 $f = 1\text{ MHz}; T_{amb} = 25\text{ }^{\circ}\text{C};$ typical values.

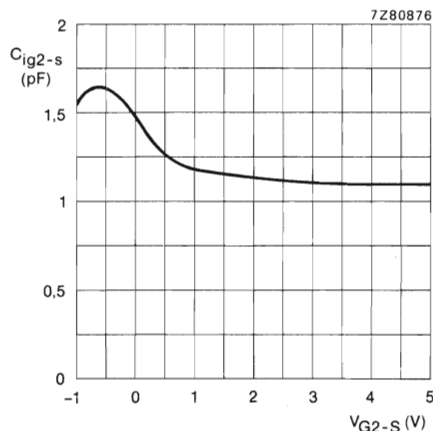


Fig. 4 $V_{G1-S} = 0\text{ V}; V_{DS} = 15\text{ V};$
 $f = 1\text{ MHz}; T_{amb} = 25\text{ }^{\circ}\text{C};$ typical values.

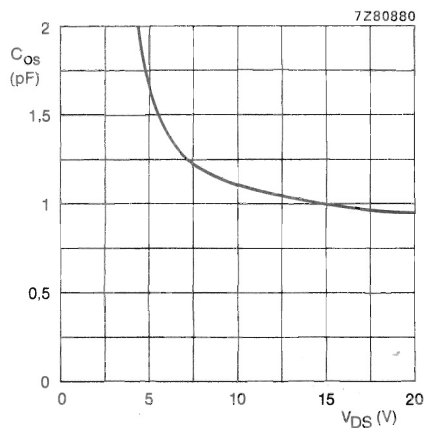


Fig. 5 $V_{G2-S} = 4 \text{ V}$; $I_D = 10 \text{ mA}$;
 $f = 1 \text{ MHz}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; typical values.

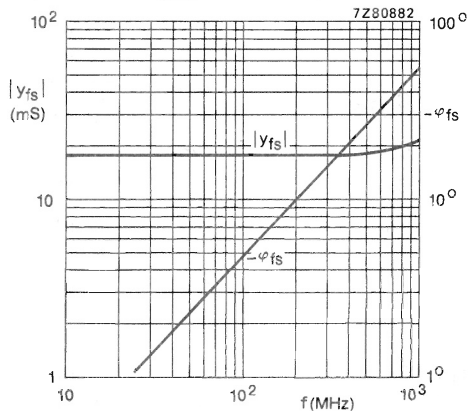


Fig. 7 $V_{G2-S} = 4 \text{ V}$; $V_{DS} = 15 \text{ V}$;
 $I_D = 10 \text{ mA}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; typical values.

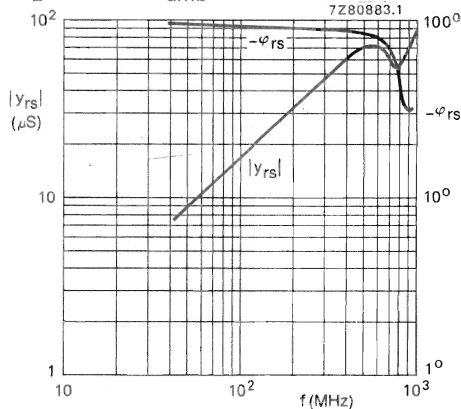


Fig. 9 $V_{G2-S} = 4 \text{ V}$; $V_{DS} = 15 \text{ V}$;
 $I_D = 10 \text{ mA}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; typical values.

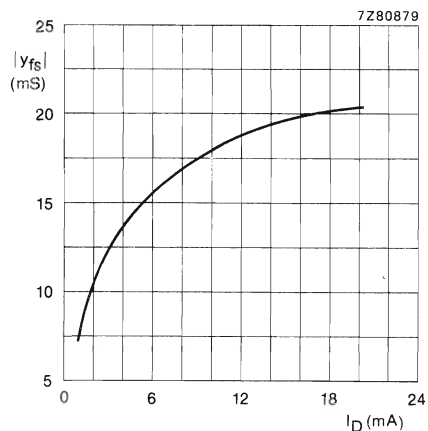


Fig. 6 $V_{G2-S} = 4 \text{ V}$; $V_{DS} = 15 \text{ V}$;
 $f = 1 \text{ kHz}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; typical values.

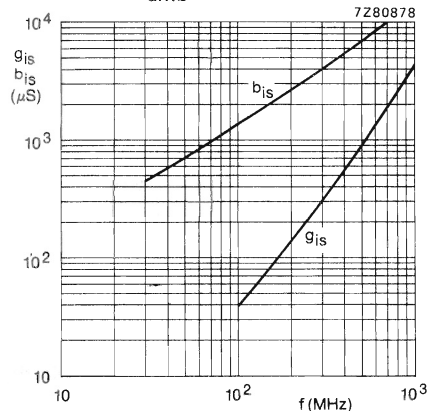


Fig. 8 $V_{G2-S} = 4 \text{ V}$; $V_{DS} = 15 \text{ V}$;
 $I_D = 10 \text{ mA}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; typical values.

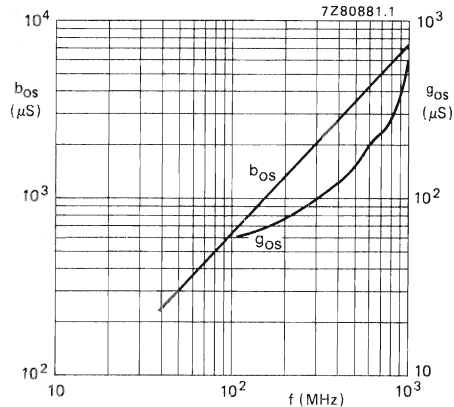


Fig. 10 $V_{G2-S} = 4 \text{ V}$; $V_{DS} = 15 \text{ V}$;
 $I_D = 10 \text{ mA}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$; typical values.

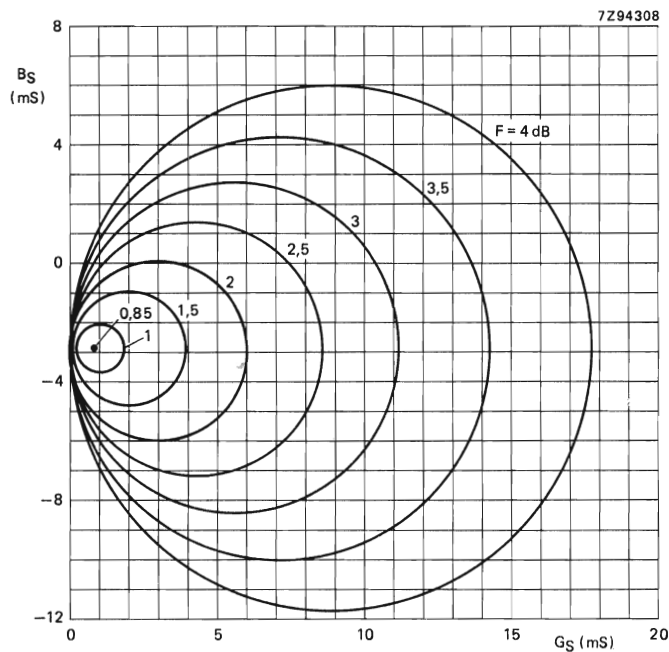


Fig. 11 $V_{G2-S} = 4$ V; $V_{DS} = 15$ V; $I_D = 10$ mA;
 $f = 200$ MHz; $T_{amb} = 25$ °C; typical values.

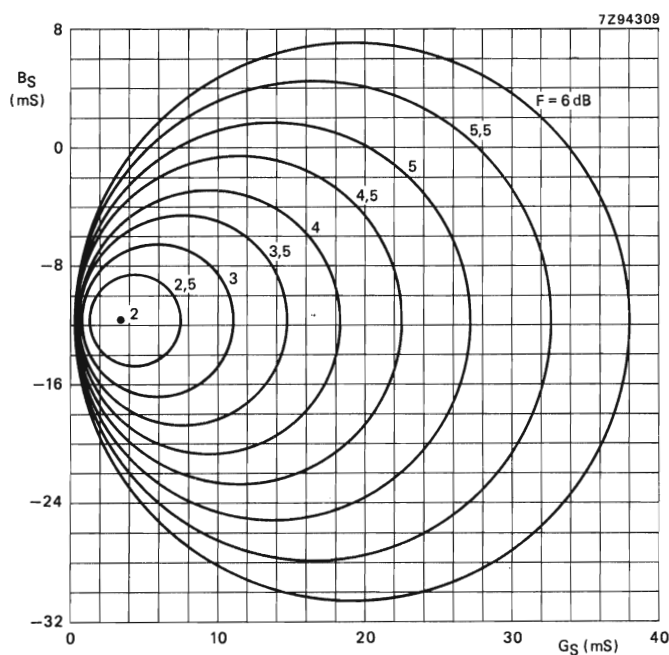


Fig. 12 $V_{G2-S} = 4$ V; $V_{DS} = 15$ V; $I_D = 10$ mA;
 $f = 800$ MHz; $T_{amb} = 25$ °C; typical values.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications, such as u.h.f. television tuners, with 12 V supply voltage.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

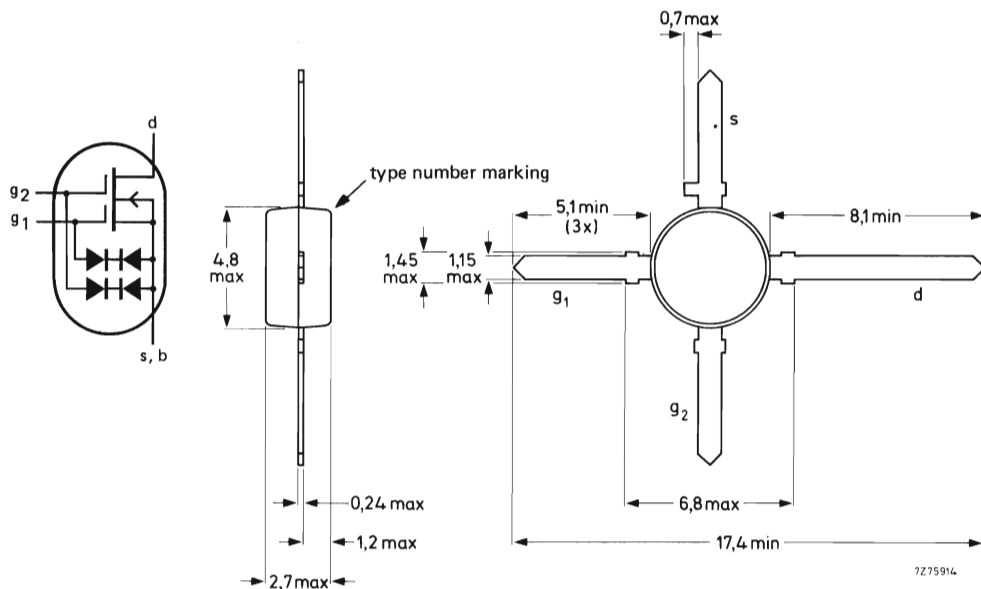
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18	V
Drain current	I_D	max.	30	mA
Total power dissipation up to $T_{amb} = 75^\circ\text{C}$	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	$^\circ\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	19	mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25	fF
Noise figure at $G_S = 5\text{ mS}$; $B_S = B_{S\text{ opt}}$ $I_D = 10\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 800\text{ MHz}$	F	typ.	2,8	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

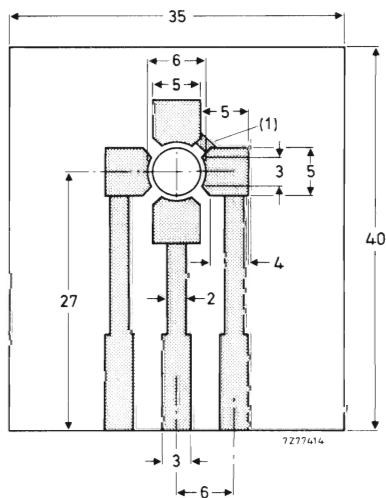
Drain-source voltage	V_{DS}	max.	18	V
Drain current (d.c. or average)	I_D	max.	30	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	225	mW
Storage temperature	T_{stg}		-65 to +150	$^{\circ}\text{C}$
Junction temperature	T_j	max.	150	$^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air
mounted on the printed-circuit board (see Fig. 2)

$$R_{th\ j-a} = 335\text{ K/W}$$

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$

Gate cut-off currents

$\pm V_{G1-S} = 7\text{ V}; V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	25 nA
$\pm V_{G2-S} = 7\text{ V}; V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	25 nA

Gate-source breakdown voltages

$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	>	8 V
$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	>	8 V

Gate-source cut-off voltages

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{(P)G1-S}$	<	1,3 V
		>	0,2 V
$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$	$-V_{(P)G2-S}$	<	1,1 V
		>	0,2 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$

Transfer admittance at $f = 1\text{ kHz}$	$ Y_{fs} $	>	17 mS
	typ.		19 mS
Input capacitance at gate 1; $f = 1\text{ MHz}$	C_{ig1-s}	<	3,0 pF
	typ.		2,6 pF
Feedback capacitance at $f = 1\text{ MHz}$	C_{rs}	<	35 fF
	typ.		25 fF
Output capacitance at $f = 1\text{ MHz}$	C_{os}	<	1,3 pF
	typ.		1,1 pF
Noise figure at $f = 800\text{ MHz}; G_S = 5\text{ mS}; B_S = B_S \text{ op1}$	F	<	3,9 dB
		typ.	2,8 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications, such as v.h.f. television tuners, f.m. tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

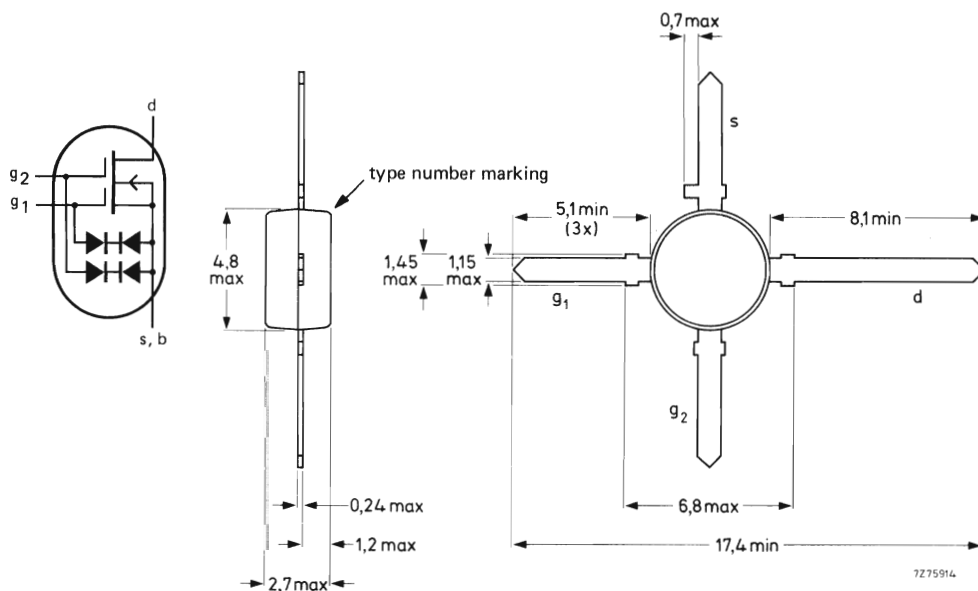
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	14 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	20 fF
Noise figure at optimum source admittance $I_D = 10\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 200\text{ MHz}$	F	typ.	0,7 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



STATIC CHARACTERISTICS $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$

$\pm I_{G1-SS} < 50\text{ nA}$

$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$

$\pm I_{G2-SS} < 50\text{ nA}$

Gate-source breakdown voltages

$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$

$\pm V_{(BR)G1-SS} > 6\text{ V}$

$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$

$\pm V_{(BR)G2-SS} > 6\text{ V}$

Drain current

$V_{DS} = 10\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$

$I_{DSS} \quad 4\text{ to }25\text{ mA}$

Gate-source cut-off voltages

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$

$-V_{(P)G1-S} < 2,5\text{ V}$

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$

$-V_{(P)G2-S} < 2,5\text{ V}$

DYNAMIC CHARACTERISTICSMeasuring conditions (common source): $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at $f = 1\text{ kHz}$

$|Y_{fs}| > 10\text{ mS}$
typ. 14 mS

Input capacitance at gate 1; $f = 1\text{ MHz}$

C_{ig1-s} typ. 2,1 pF

Input capacitance at gate 2; $f = 1\text{ MHz}$

C_{ig2-s} typ. 1,0 pF

Feedback capacitance at $f = 1\text{ MHz}$

C_{rs} typ. 20 fF

Output capacitance at $f = 1\text{ MHz}$

C_{os} typ. 1,1 pF

Noise figure at $f = 100\text{ MHz}; G_S = 1\text{ mS}; B_S = B_S\text{ opt}$

F typ. 0,7 dB
< 1,7 dB

Noise figure at $f = 200\text{ MHz}; G_S = 2\text{ mS}; B_S = B_S\text{ opt}$

F typ. 1,0 dB
< 2,0 dB

Transducer gain at $f = 100\text{ MHz}; G_S = 1\text{ mS}; B_S = B_S\text{ opt};$

$G_L = 0,5\text{ mS}; B_L = B_L\text{ opt}$

G_{tr} typ. 29 dB ←

Transducer gain at $f = 200\text{ MHz}; G_S = 2\text{ mS}; B_S = B_S\text{ opt};$

$G_L = 0,5\text{ mS}; B_L = B_L\text{ opt}$

G_{tr} typ. 26 dB ←

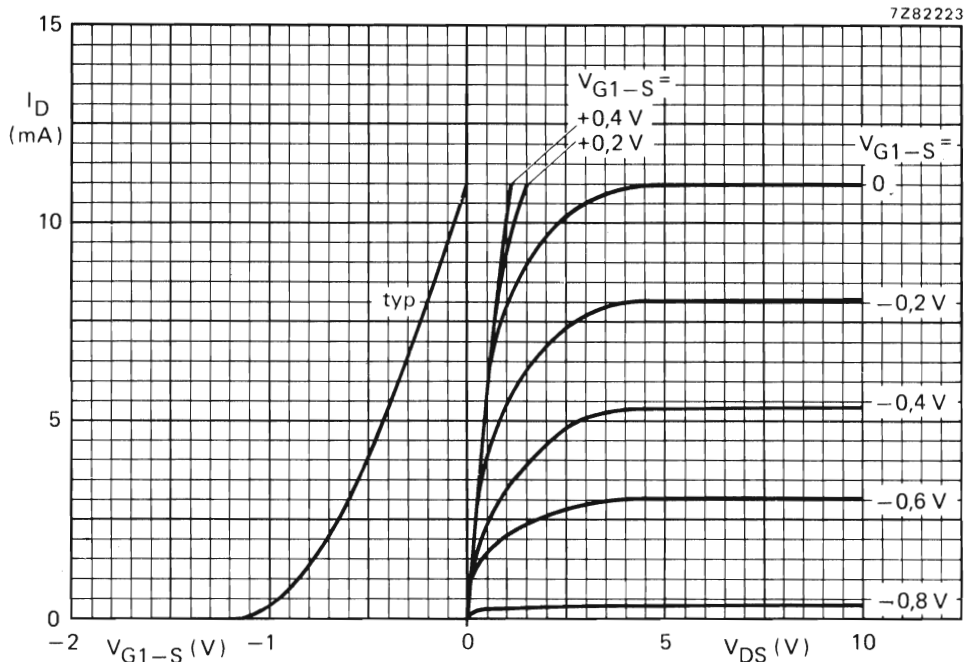


Fig. 3 Left-hand graph: $V_{DS} = 10$ V; $V_{G2-S} = +4$ V; $T_{amb} = 25$ °C. Right-hand graph: $V_{G2-S} = +4$ V; $T_{amb} = 25$ °C.

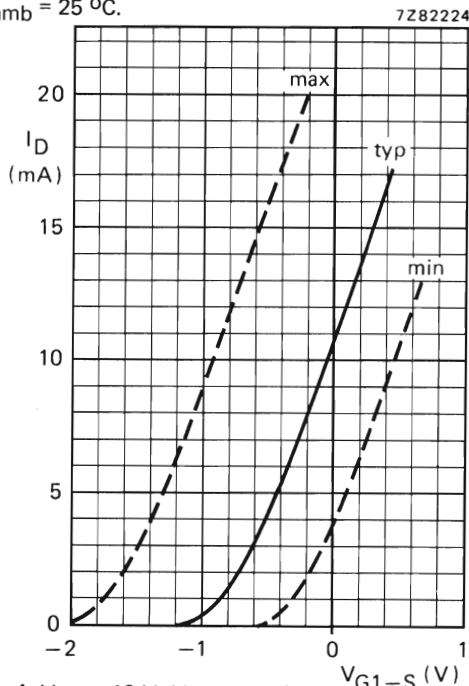


Fig. 4 $V_{DS} = 10$ V; $V_{G2-S} = +4$ V; $T_{amb} = 25$ °C.

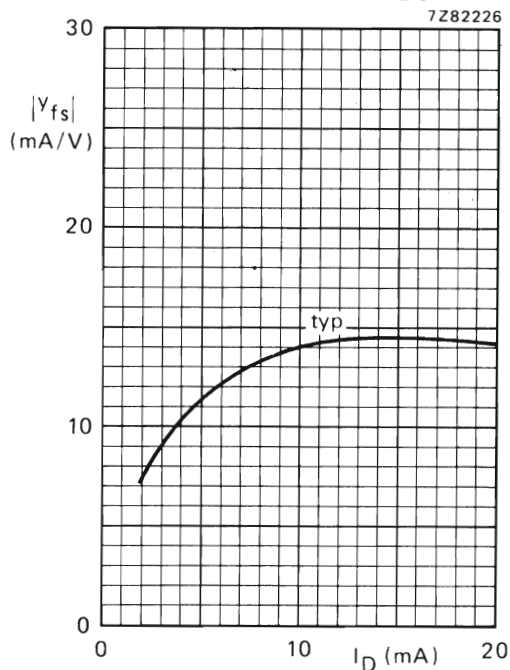


Fig. 5 $V_{DS} = 10$ V; $V_{G2-S} = +4$ V; $f = 1$ kHz; $T_{amb} = 25$ °C.

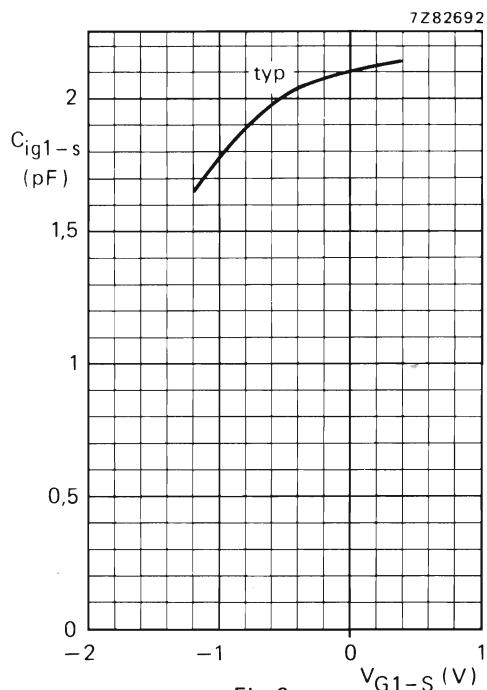


Fig. 6.

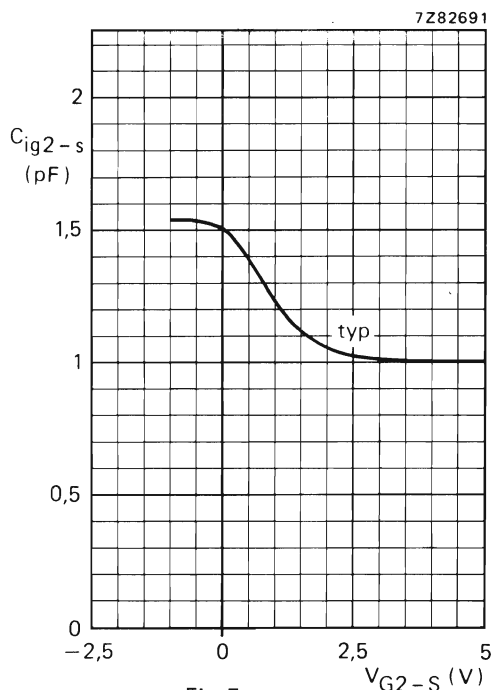


Fig. 7.

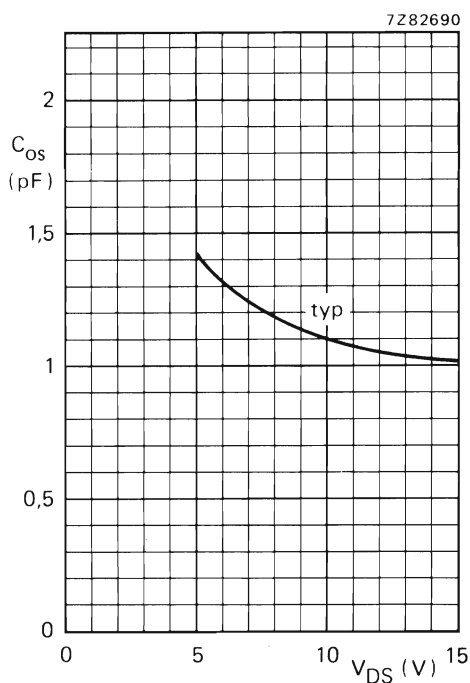


Fig. 8.

Measuring conditions:

Fig. 6 $V_{DS} = 10$ V; $V_{G2-S} = +4$ V; $f = 1$ MHz;
 $T_{amb} = 25$ °C.

Fig. 7 $V_{DS} = 10$ V; $V_{G1-S} = 0$; $f = 1$ MHz;
 $T_{amb} = 25$ °C.

Fig. 8 $V_{G2-S} = +4$ V; $I_D = 10$ mA; $f = 1$ MHz;
 $T_{amb} = 25$ °C.

Measuring conditions for Figs 9 to 12: $V_{DS} = 10\text{ V}$; $I_D = 10\text{ mA}$; $V_{G2-S} = +4\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

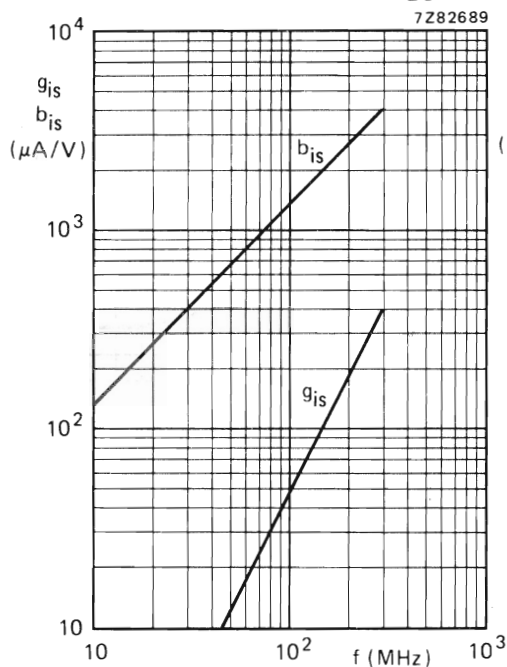


Fig. 9.

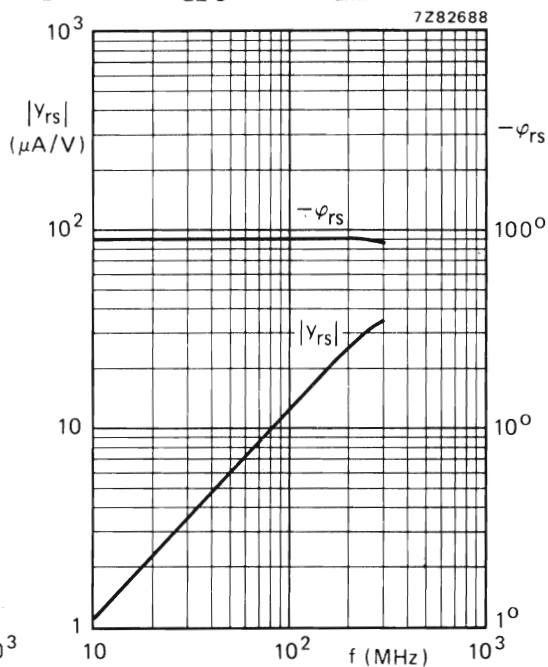


Fig. 10.

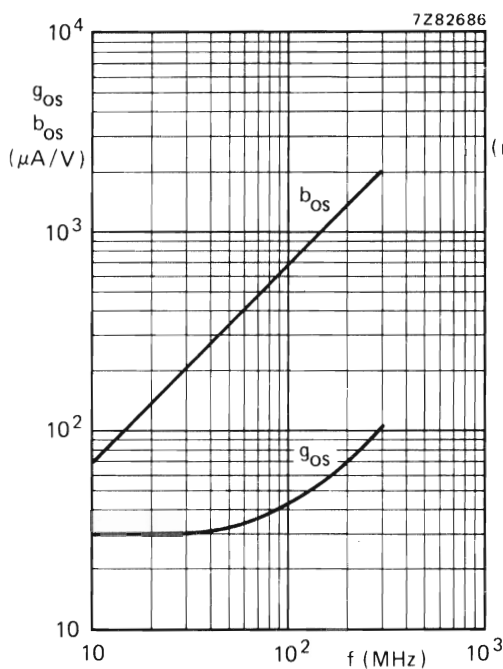


Fig. 11.

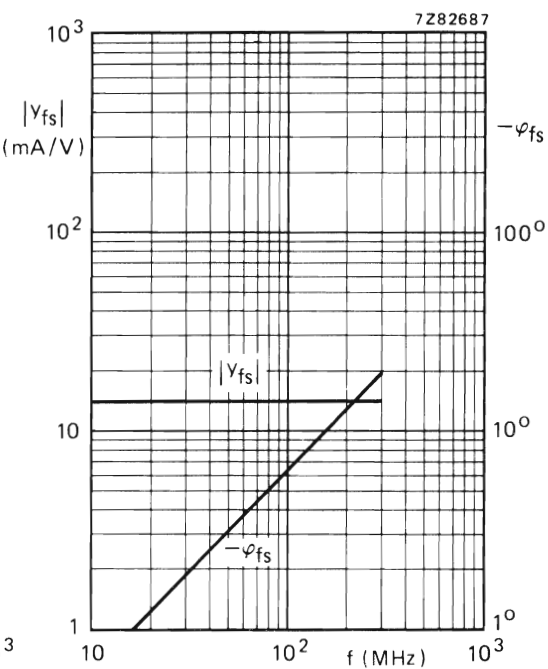


Fig. 12.

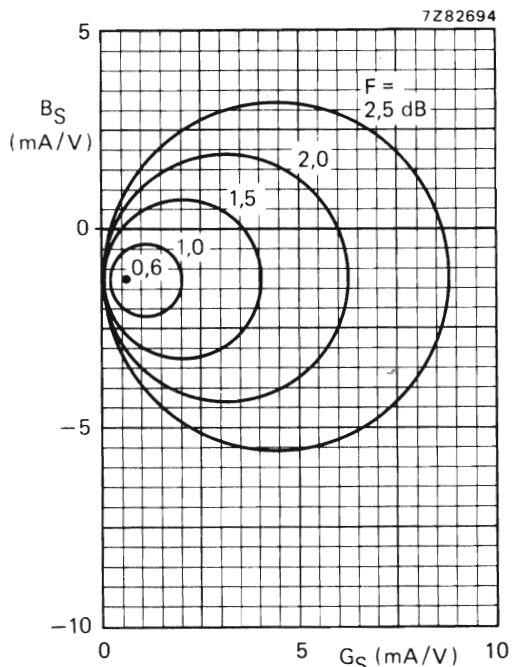


Fig. 13 $V_{DS} = 10$ V; $V_{G2S} = +4$ V; $I_D = 10$ mA;
 $f = 100$ MHz; $T_{amb} = 25$ °C; circles of typical
 constant noise figures.

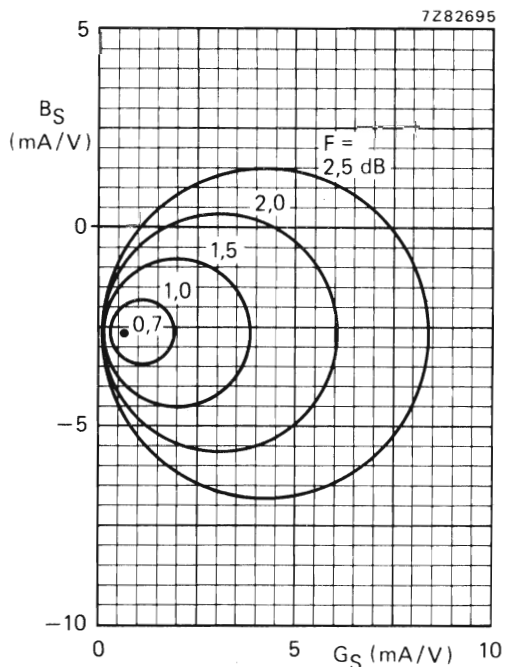


Fig. 14 $V_{DS} = 10$ V; $V_{G2S} = +4$ V; $I_D = 10$ mA;
 $f = 200$ MHz; $T_{amb} = 25$ °C; circles of typical
 constant noise figures.

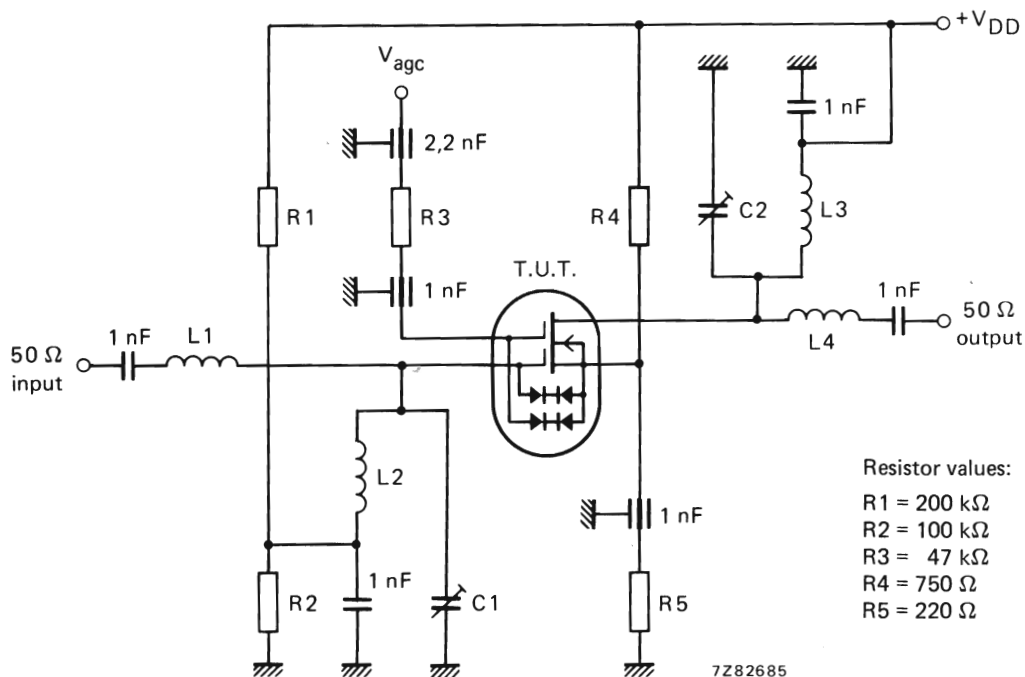


Fig. 15 Automatic gain control test circuit at $f = 200 \text{ MHz}$ (see also Fig. 16).

$V_{DD} = 16 \text{ V}$; $G_S = 2 \text{ mA/V}$; $G_L = 0,5 \text{ mA/V}$.

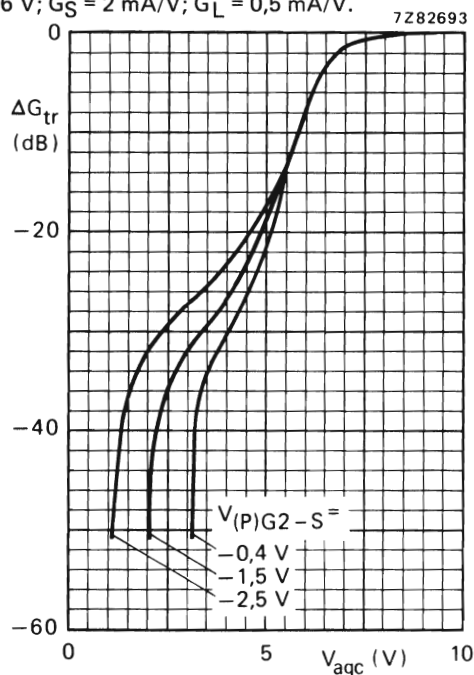


Fig. 16 $V_{DD} = 16 \text{ V}$; $f = 200 \text{ MHz}$;
 $T_{amb} = 25 \text{ }^\circ\text{C}$; typical values;
 see also Fig. 15.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications, such as v.h.f. television tuners, f.m. tuners, with 12 V supply voltage.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

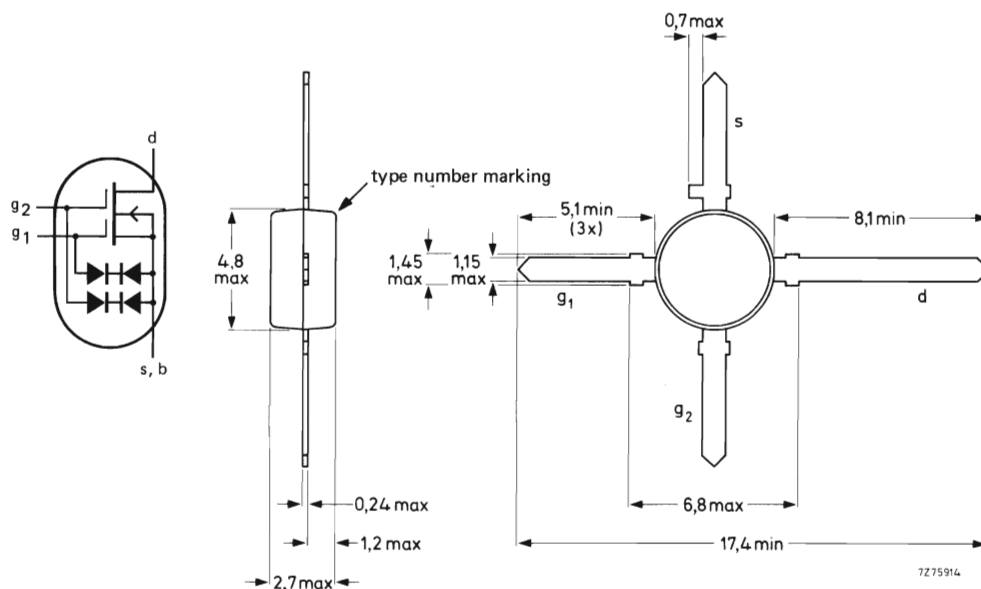
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	40 mA
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 15\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	25 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 15\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	30 fF
Noise figure at $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$ $I_D = 15\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 200\text{ MHz}$	F	typ.	1,2 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

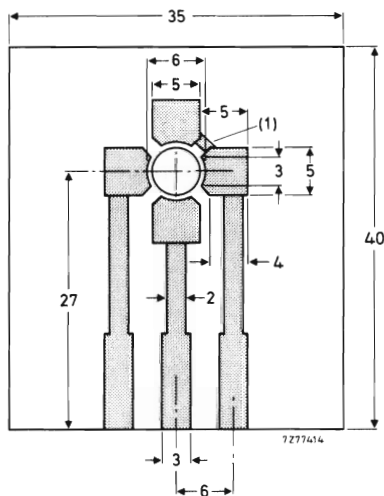
Drain-source voltage	V_{DS}	max.	20 V
Drain current (d.c. or average)	I_D	max.	40 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 75\text{ }^{\circ}\text{C}$	P_{tot}	max.	225 mW
Storage temperature	T_{stg}		-65 to +150 $^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air
 mounted on the printed-circuit board (see Fig. 2)

$$R_{thj-a} = 335\text{ K/W}$$

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS $T_{amb} = 25\text{ }^{\circ}\text{C}$

Gate cut-off currents

$\pm V_{G1-S} = 7\text{ V}; V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	25 nA
$\pm V_{G2-S} = 7\text{ V}; V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	25 nA

Gate-source breakdown voltages

$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	>	8 V
$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	>	8 V

Gate-source cut-off voltages

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{(P)G1-S}$	<	1,3 V
$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$	$-V_{(P)G2-S}$	<	1,1 V

DYNAMIC CHARACTERISTICSMeasuring conditions (common source): $I_D = 15\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$

Transfer admittance at $f = 1\text{ kHz}$	$ y_{fs} $	>	20 mS
		typ.	25 mS
Input capacitance at gate 1; $f = 1\text{ MHz}$	C_{ig1-s}	typ.	4,0 pF
Input capacitance at gate 2; $f = 1\text{ MHz}$	C_{ig2-s}	typ.	1,7 pF
Feedback capacitance at $f = 1\text{ MHz}$	C_{rs}	typ.	30 fF
Output capacitance at $f = 1\text{ MHz}$	C_{os}	typ.	2,0 pF
Noise figure at $f = 200\text{ MHz}; G_S = 2\text{ mS}; B_S = B_S\text{ opt}$	F	typ.	1,2 dB



SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT-143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in u.h.f. applications in television tuners. The device is also suitable for use in professional communication equipment.

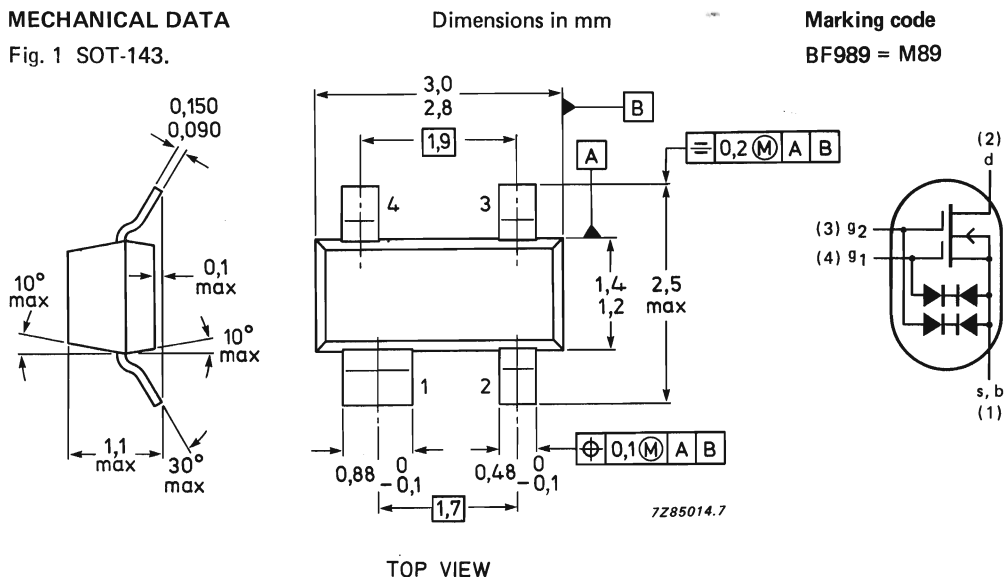
The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current (peak value)	I_{DM}	max.	30 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}$	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 7\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	12 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 7\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25 fF
Noise figure at $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$ $I_D = 7\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 800\text{ MHz}$	F	typ.	2,8 dB

MECHANICAL DATA

Fig. 1 SOT-143.



See also *Soldering recommendations*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (d.c. or average)	I_D	max.	20 mA
Drain current (peak value)	I_{DM}	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		-65 to +150 $^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j-a}$	\approx	460 K/W
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STATIC CHARACTERISTICS $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	$<$	50 nA
$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	$<$	50 nA

Drain current

$V_{DS} = 10\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$	I_{DSS}		2 to 20 mA
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Gate-source breakdown voltages

$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		6 to 20 V
$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		6 to 20 V

Gate-source cut-off voltages

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{(P)G1-S}$	$<$	2,7 V
$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$	$-V_{(P)G2-S}$	$<$	2,7 V

DYNAMIC CHARACTERISTICSMeasuring conditions (common source): $I_D = 7\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$

Transfer admittance at $f = 1\text{ kHz}$	$ Y_{fs} $	$>$	9,5 mS
		typ.	12 mS
Input capacitance at gate 1; $f = 1\text{ MHz}$	C_{ig1-s}	typ.	1,8 pF
Input capacitance at gate 2; $f = 1\text{ MHz}$	C_{ig2-s}	typ.	1,0 pF
Feedback capacitance at $f = 1\text{ MHz}$	C_{rs}	typ.	25 fF
Output capacitance at $f = 1\text{ MHz}$	C_{os}	typ.	0,9 pF
→ Noise figure at $G_S = 2\text{ mS}; B_S = B_S\text{ opt}$			
$f = 200\text{ MHz}$	F	typ.	1,6 dB
$f = 800\text{ MHz}$	F	typ.	2,8 dB

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope with source and substrate interconnected, intended for u.h.f. applications, such as u.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Total power dissipation up to $T_{amb} = 60^{\circ}\text{C}$	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150°C
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	19 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25 fF
Noise figure at optimum source admittance $I_D = 10\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 800\text{ MHz}$	F	typ.	2,8 dB

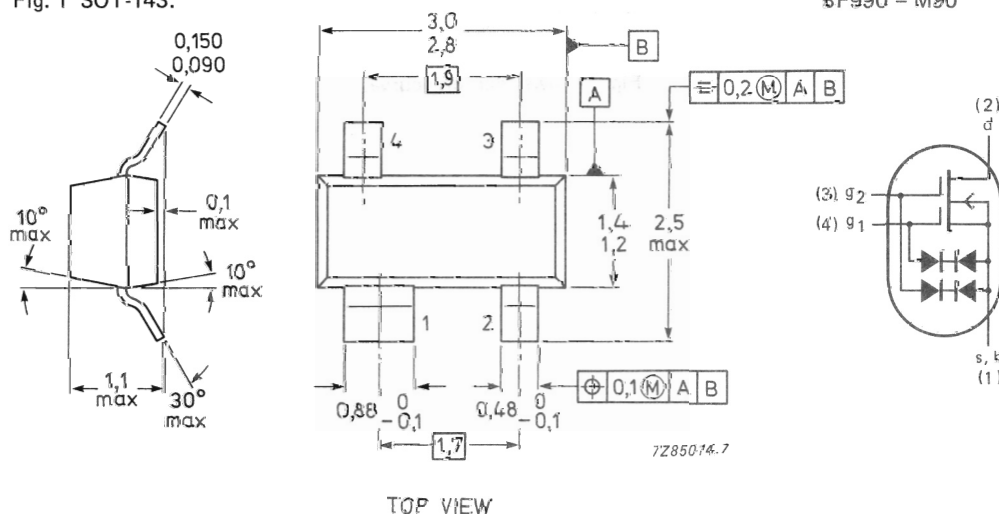
MECHANICAL DATA

Fig. 1 SOT-143.

Dimensions in mm

Marking code

BF990 = M90



See also *Soldering recommendations*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	200 mW
Storage temperature	T_{stg}	max.	$-65\text{ to }+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	$150\text{ }^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air*	R_{thj-a}	=	460 K/W
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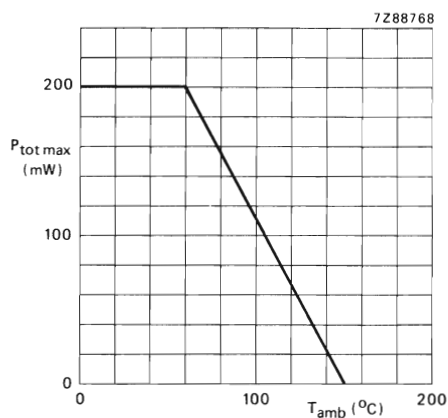


Fig. 2 Power derating curve.

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

STATIC CHARACTERISTICS $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

gate 1;

$\pm V_{G1-S} = 7\text{ V}; V_{G2-S} = V_{DS} = 0$

$\pm I_{G1-SS} < 25\text{ nA}$

gate 2;

$\pm V_{G2-S} = 7\text{ V}; V_{G1-S} = V_{DS} = 0$

$\pm I_{G2-SS} < 25\text{ nA}$

Gate-source breakdown voltages

gate 1;

$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$

$\pm V_{(BR)G1-SS} > 8\text{ V}$

gate 2;

$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$

$\pm V_{(BR)G2-SS} > 8\text{ V}$

Gate-source cut-off voltages

gate 1;

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$

$-V_{(P)G1-S} < 1,3\text{ V}$

gate 2;

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$

$-V_{(P)G2-S} < 1,1\text{ V}$

DYNAMIC CHARACTERISTICSMeasuring conditions (common source): $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at $f = 1\text{ kHz}$

$|y_{fs}| > 17\text{ mS}$
typ. 19 mS

Input capacitance at gate 1; $f = 1\text{ MHz}$

$C_{ig1-s} < 3,0\text{ pF}$

Input capacitance at gate 2; $f = 1\text{ MHz}$

$C_{ig2-s} \text{ typ. } 1,4\text{ pF}$

Feedback capacitance at $f = 1\text{ MHz}$

$C_{rs} \text{ typ. } 25\text{ fF}$

Output capacitance at $f = 1\text{ MHz}$

$C_{os} \text{ typ. } 1,2\text{ pF}$

Noise figure at $f = 800\text{ MHz}; G_S = 5\text{ mS}; B_S = B_S \text{ opt}$

$F \text{ typ. } 2,8\text{ dB}$

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT-143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners and f.m. tuners. The device is also suitable for use in professional communication equipment.

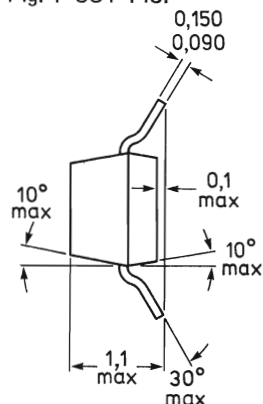
The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

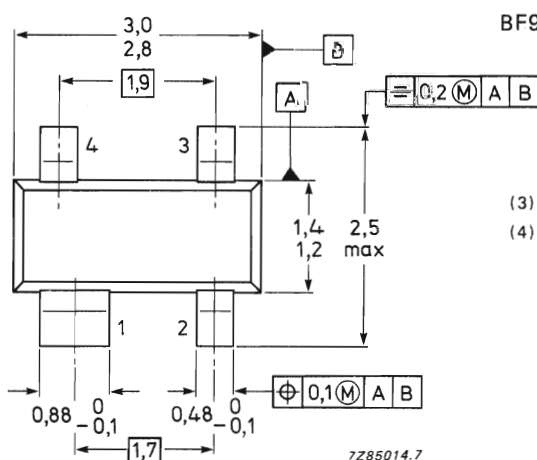
Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}$	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	14 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	20 fF
Noise figure at optimum source admittance $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; f = 200\text{ MHz}$	F	typ.	0,7 dB

MECHANICAL DATA

Fig. 1 SOT-143.

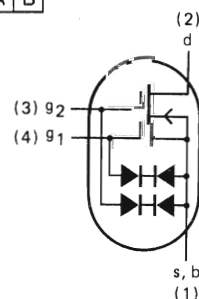


Dimensions in mm



Marking code

BF991 = M91



TOP VIEW

See also *Soldering recommendations*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (d.c. or average)	I_D	max.	20 mA
Drain current (peak value)	I_{DM}	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		-65 to $+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	$150\text{ }^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j-a}$	=	460 K/W
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STATIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	50 nA
$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	50 nA

Drain current

$V_{DS} = 10\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$	I_{DSS}		4 to 25 mA
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Gate-source breakdown voltages

$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	>	6 V
$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	>	6 V

Gate-source cut-off voltages

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{(P)G1-S}$	<	2,5 V
$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$	$-V_{(P)G2-S}$	<	2,5 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$

Transfer admittance at $f = 1\text{ kHz}$	$ Y_{fs} $	>	10 mS
		typ.	14 mS
Input capacitance at gate 1; $f = 1\text{ MHz}$	C_{ig1-s}	typ.	2,1 pF
Input capacitance at gate 2; $f = 1\text{ MHz}$	C_{ig2-s}	typ.	1,0 pF
Feedback capacitance at $f = 1\text{ MHz}$	C_{rs}	typ.	20 fF
Output capacitance at $f = 1\text{ MHz}$	C_{os}	typ.	1,1 pF
Noise figure		typ.	0,7 dB
→ $f = 100\text{ MHz}; G_S = 1\text{ mS}; B_S = B_S\text{ opt}$	F	<	1,7 dB
→ $f = 200\text{ MHz}; G_S = 2\text{ mS}; B_S = B_S\text{ opt}$	F	typ.	1,0 dB
		<	2,0 dB
Transducer gain **			
→ $f = 100\text{ MHz}; G_S = 1\text{ mS}; B_S = B_S\text{ opt};$ $G_L = 0,5\text{ mS}; B_L = B_L\text{ opt}$	G_{tr}	typ.	29 dB
→ $f = 200\text{ MHz}; G_S = 2\text{ mS}; B_S = B_S\text{ opt};$ $G_L = 0,5\text{ mS}; B_L = B_L\text{ opt}$	G_{tr}	typ.	26 dB

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

** Crystal mounted in a SOT-103 envelope.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT-143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

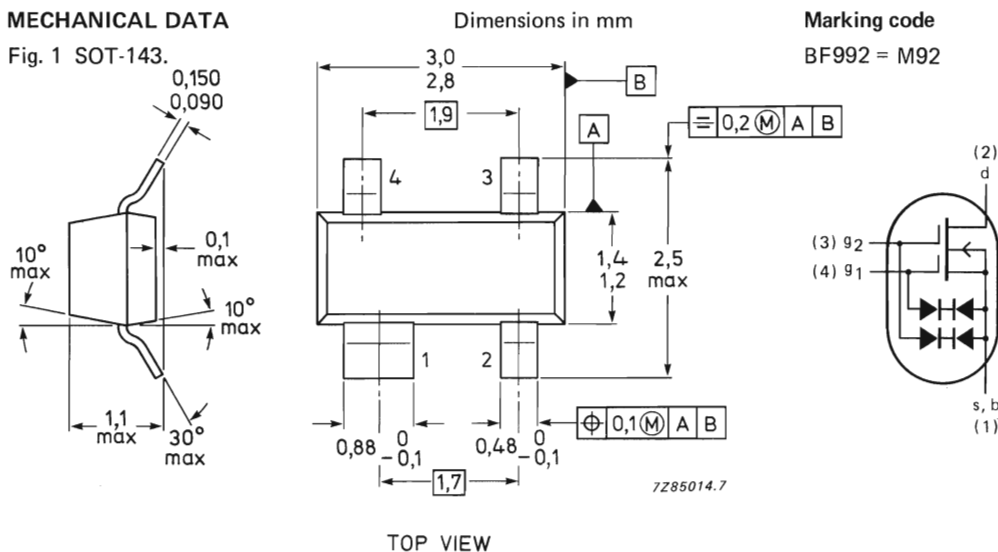
The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	40 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}$	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 15\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	25 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 15\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	30 fF
Noise figure at $G_S = 2\text{ mS}$ $I_D = 15\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 200\text{ MHz}$	F	typ.	1,2 dB

MECHANICAL DATA

Fig. 1 SOT-143.



See also *Soldering recommendations*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (d.c. or average)	I_D	max.	40 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		-65 to $+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	$150\text{ }^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j-a}$	=	460 K/W
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STATIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

$\pm V_{G1-S} = 7\text{ V}; V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	25 nA
$\pm V_{G2-S} = 7\text{ V}; V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	25 nA

Gate-source breakdown voltages

$\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	>	8 V
$\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	>	8 V

Gate-source cut-off voltages

$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{(P)G1-S}$	0,2 to 1,3 V
$I_D = 20\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$	$-V_{(P)G2-S}$	0,2 to 1,1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 15\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$

Transfer admittance at $f = 1\text{ kHz}$	$ y_{fs} $	>	20 mS
		typ.	25 mS
Input capacitance at gate 1; $f = 1\text{ MHz}$	C_{ig1-s}	typ.	4 pF
Input capacitance at gate 2; $f = 1\text{ MHz}$	C_{ig2-s}	typ.	1,7 pF
Feedback capacitance at $f = 1\text{ MHz}$	C_{rs}	typ.	30 fF
		<	40 fF
Output capacitance at $f = 1\text{ MHz}$	C_{os}	typ.	2 pF
Noise figure at $f = 200\text{ MHz}; G_S = 2\text{ mS}$	F	typ.	1,2 dB

→ * Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope with source and substrate interconnected, intended for u.h.f. and v.h.f. applications, such as u.h.f./v.h.f. television tuners and professional communication equipment.

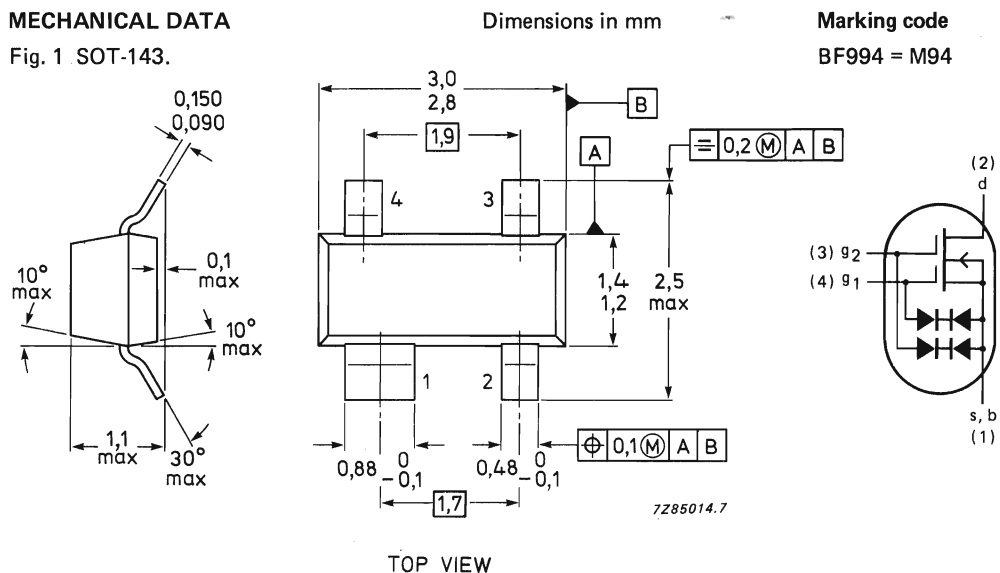
This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}$	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	17 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25 fF
Noise figure at optimum source admittance $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 200\text{ MHz}$	F	typ.	1,5 dB

MECHANICAL DATA

Fig. 1 SOT-143.



See also *Soldering recommendations*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	200 mW
Storage temperature	T_{stg}	-65 to + 150 $^{\circ}\text{C}$	
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air*	R_{thj-a}	=	460 K/W
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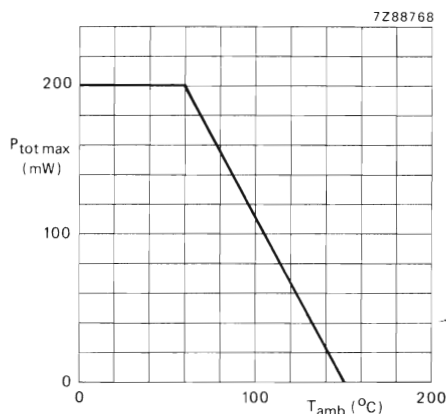


Fig. 2 Power derating curve.

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,6 mm.

STATIC CHARACTERISTICS $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

gate 1; $\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	50 nA
gate 2; $\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	50 nA

Gate-source breakdown voltages

gate 1; $\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		6 to 20 V
gate 2; $\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		6 to 20 V

Gate-source cut-off voltages

gate 1; $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{(P)G1-S}$	<	2,5 V
gate 2; $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; V_{G1-S} = 0$	$-V_{(P)G2-S}$	<	2,0 V

Drain-source cut-off voltage

$V_{DS} = 15\text{ V}; V_{G2-S} = 4\text{ V}$	I_{DSS}		2 to 20 mA
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DYNAMIC CHARACTERISTICSMeasuring conditions (common source): $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$

Transfer admittance at $f = 1\text{ kHz}$	$ Y_{fs} $	>	15 mS	
		typ.	17 mS	
Input capacitance at gate 1; $f = 1\text{ MHz}$	C_{ig1-s}	typ.	2,5 pF	
Input capacitance at gate 2; $f = 1\text{ MHz}$	C_{ig2-s}	typ.	1,2 pF	
Feedback capacitance at $f = 1\text{ MHz}$	C_{rs}	typ.	25 fF	
Output capacitance at $f = 1\text{ MHz}$	C_{os}	typ.	1,0 pF	
Noise figure at $f = 200\text{ MHz}; G_S = 2\text{ mS}; B_S = B_S\text{ opt}$	F	typ.	1,5 dB	←
		<	2,8 dB	
Power gain at $G_S = 2\text{ mS}; B_S = B_S\text{ opt}$				←
$G_L = 0,5\text{ mS}; B_L = B_L\text{ opt}; f = 200\text{ MHz}$	G_p	typ.	25 dB	←

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope (SOT-143) with source and substrate interconnected and intended for v.h.f. applications in television tuners, using SMD* technology. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

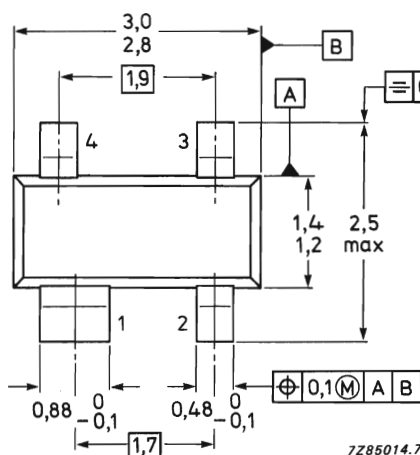
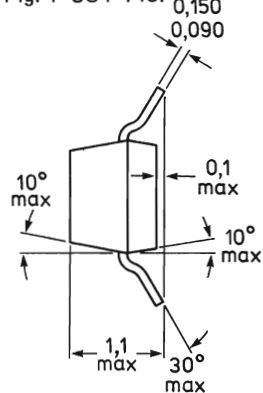
* Surface Mounted Devices.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	50 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	18 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25 fF
Noise figure at $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 200\text{ MHz}$	F	typ.	1,0 dB

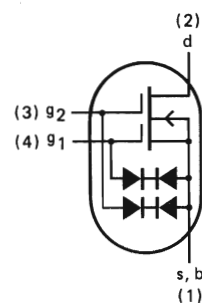
MECHANICAL DATA

Fig. 1 SOT-143.



TOP VIEW

Dimensions in mm
Marking code
BF994S = M93



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (d.c. or average)	I_D	max.	50 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
Storage temperature	T_{stg}		-65 to $150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	$150\text{ }^{\circ}\text{C}$

THERMAL RESISTANCEFrom junction to ambient in free air mounted on
a ceramic substrate of 8 mm x 10 mm x 0,7 mm

$R_{th\ j-a}$	=	430 K/W
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STATIC CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

 $\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$ $\pm I_{G1-S} < 50\text{ nA}$ $\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$ $\pm I_{G2-S} < 50\text{ nA}$

Gate-source breakdown voltages

 $\pm I_{G1-S} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$ $\pm V_{(BR)G1-SS} 6,0\text{ to }20\text{ V}$ $\pm I_{G2-S} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$ $\pm V_{(BR)G2-SS} 6,0\text{ to }20\text{ V}$

Drain current

 $V_{DS} = 15\text{ V}; V_{G1-S} = 0; V_{G2-S} = 4\text{ V}$ $I_{DSS} 4\text{ to }20\text{ mA}$

Gate-source cut-off voltages

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$ $-V_{(P)G1-S} < 2,5\text{ V}$ $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; V_{G1-S} = 0$ $-V_{(P)G2-S} < 2,0\text{ V}$ **DYNAMIC CHARACTERISTICS**Measuring conditions (common source): $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$.Transfer admittance at $f = 1\text{ kHz}$

$ y_{fs} $	$>$	15 mS
	typ.	18 mS

Input capacitance at gate 1: $f = 1\text{ MHz}$

C_{ig1-s}	typ.	2,5 pF
	$<$	3,0 pF

Input capacitance at gate 2: $f = 1\text{ MHz}$

C_{ig2-s}	typ.	1,2 pF
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Feedback capacitance at $f = 1\text{ MHz}$

C_{rs}	typ.	25 fF
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Output capacitance at $f = 1\text{ MHz}$

C_{os}	typ.	1,0 pF
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→ Noise figure at $G_S = 2\text{ mS}; B_S = B_S\text{ opt}; f = 200\text{ MHz}$

F	typ.	1,0 dB
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→ Power gain at $G_S = 2\text{ mS}; B_S = B_S\text{ opt}$ $G_L = 0,5\text{ mS}; B_L = B_L\text{ opt}; f = 200\text{ MHz}$

G_p	typ.	25 dB
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SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope, with source and substrate interconnected, intended for u.h.f. applications, such as television tuners and professional communication equipment.

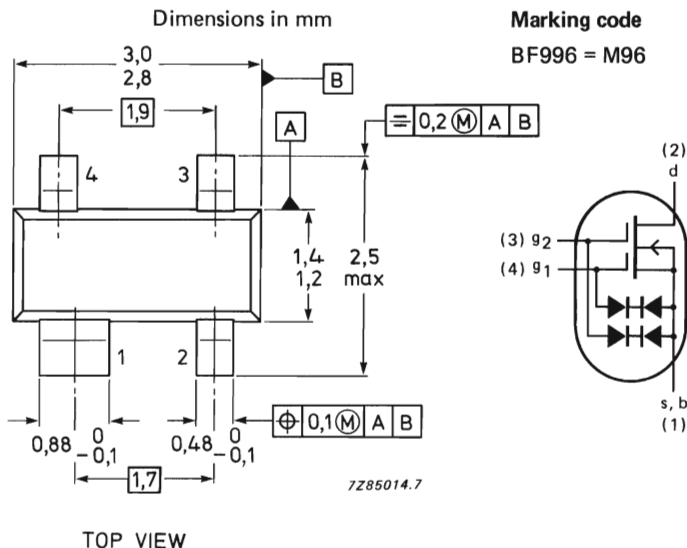
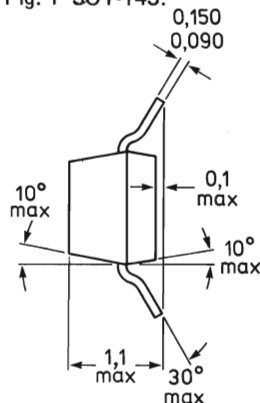
This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}$	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	17 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25 fF
Noise figure at optimum source admittance $I_D = 10\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 800\text{ MHz}$	F	typ.	2,8 dB
$I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 200\text{ MHz}$	F	typ.	1,5 dB

MECHANICAL DATA

Fig. 1 SOT-143.



See also *Soldering recommendations*.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		$-65\text{ to }+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	$150\text{ }^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air*	R_{thj-a}	=	460 K/W
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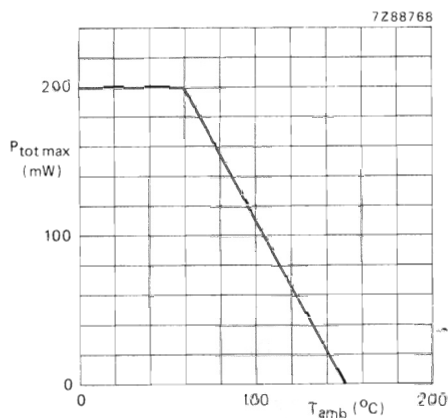


Fig. 2 Power derating curve.

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

STATIC CHARACTERISTICS $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

gate 1;

 $\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$ $\pm I_{G1-SS}$ < 50 nA

gate 2;

 $\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$ $\pm I_{G2-SS}$ < 50 nA

Gate-source breakdown voltages

gate 1;

 $\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$ $\pm V_{(BR)G1-SS}$ 6 to 20 V

gate 2;

 $\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$ $\pm V_{(BR)G2-SS}$ 6 to 20 V

Gate-source cut-off voltages

gate 1;

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$ $-V_{(P)G1-S}$ < 2,5 V

gate 2;

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; V_{G1-S} = 0$ $-V_{(P)G2-S}$ < 2,0 V

Drain-source cut-off voltage

 $V_{DS} = 15\text{ V}; V_{G2-S} = 4\text{ V}$ I_{DSS} 2 to 20 mA**DYNAMIC CHARACTERISTICS**Measuring conditions (common source): $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ Transfer admittance at $f = 1\text{ kHz}$ $|Y_{fs}|$ > 15 mS
typ. 17 mSInput capacitance at gate 1; $f = 1\text{ MHz}$ C_{ig1-s} typ. 2,2 pFInput capacitance at gate 2; $f = 1\text{ MHz}$ C_{ig2-s} typ. 1,1 pFFeedback capacitance at $f = 1\text{ MHz}$ C_{rs} typ. 25 fFOutput capacitance at $f = 1\text{ MHz}$ C_{os} typ. 0,8 pF

Noise figure

at $G_S = 2\text{ mS}; B_S = B_S\text{ opt}; f = 200\text{ MHz}$ F typ. 1,5 dBat $G_S = 2\text{ mS}; B_S = B_S\text{ opt}; f = 800\text{ MHz}$ F typ. 2,8 dB
< 3,9 dB

Power gain

 $G_S = 2\text{ mS}; B_S = B_S\text{ opt}; G_L = 0,5\text{ mS};$ $B_L = B_L\text{ opt}; f = 200\text{ MHz}$ G_p typ. 25 dB $G_S = 2\text{ mS}; B_S = B_S\text{ opt}; G_L = 1,0\text{ mS};$ $B_L = B_L\text{ opt}; f = 800\text{ MHz}$ G_p typ. 18 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope (SOT-143) with source and substrate interconnected and intended for u.h.f. applications in television tuners, using SMD* technology. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

* Surface Mounted Devices

QUICK REFERENCE DATA

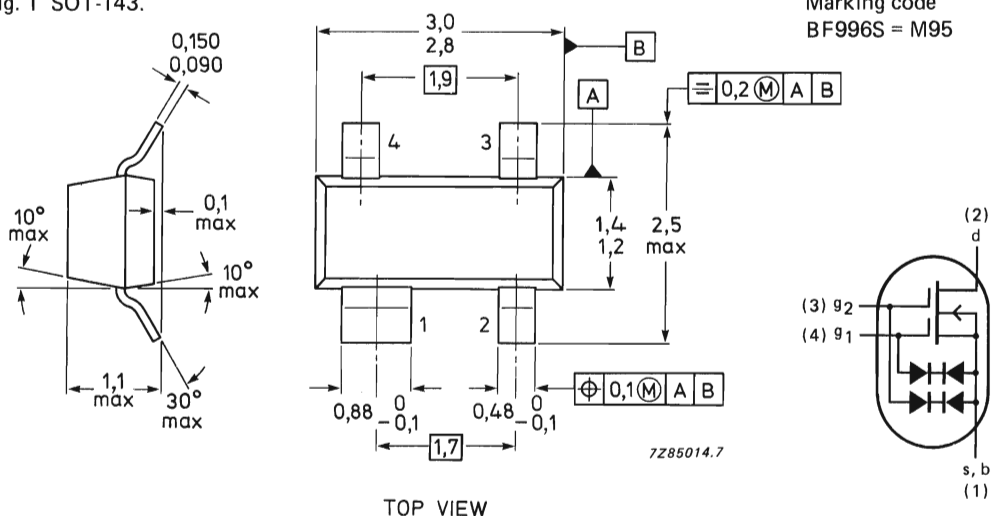
Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	18 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25 fF
Noise figure at $G_S = 3,3\text{ mS}$; $B_S = B_{S\text{ opt}}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 800\text{ MHz}$	F	typ.	1,8 dB

MECHANICAL DATA

Fig. 1 SOT-143.

Dimensions in mm

Marking code
BF996S = M95



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (d.c. or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
Storage temperature	T_{stg}		-65 to 150 $^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air mounted on
a ceramic substrate of 8 mm x 10 mm x 0,7 mm

$R_{th\ j-a}$	=	430 K/W
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STATIC CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

$\pm V_{G1-S} = 5\text{ V}$; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-S}$	<	50 nA
$\pm V_{G2-S} = 5\text{ V}$; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-S}$	<	50 nA

Gate-source breakdown voltages

$\pm I_{G1-S} = 10\text{ mA}$; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	6,0 to 20 V
$\pm I_{G2-S} = 10\text{ mA}$; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	6,0 to 20 V

Drain current

$V_{DS} = 15\text{ V}$; $V_{G1-S} = 0$; $V_{G2-S} = 4\text{ V}$	I_{DSS}	4 to 20 mA
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Gate-source cut-off voltages

$I_D = 20\text{ }\mu\text{A}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$-V_{(P)G1-S}$	<	2,5 V
$I_D = 20\text{ }\mu\text{A}$; $V_{DS} = 15\text{ V}$; $V_{G1-S} = 0$	$-V_{(P)G2-S}$	<	2,0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Transfer admittance at $f = 1\text{ kHz}$	$ y_{fs} $	>	15 mS
		typ.	18 mS
Input capacitance at gate 1: $f = 1\text{ MHz}$	C_{ig1-s}	typ.	2,3 pF
		<	2,6 pF
Input capacitance at gate 2: $f = 1\text{ MHz}$	C_{ig2-s}	typ.	1,2 pF
Feedback capacitance at $f = 1\text{ MHz}$	C_{rs}	typ.	25 fF
Output capacitance at $f = 1\text{ MHz}$	C_{os}	typ.	0,8 pF

→ Noise figure

$f = 200\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$	F	typ.	1,0 dB
$f = 800\text{ MHz}$; $G_S = 3,3\text{ mS}$; $B_S = B_{S\text{ opt}}$		typ.	1,8 dB

→ Power gain

$f = 200\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 0,5\text{ mS}$; $B_L = B_{L\text{ opt}}$	G_p	typ.	25 dB
$f = 800\text{ MHz}$; $G_S = 3,3\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 1,0\text{ mS}$; $B_L = B_{L\text{ opt}}$		typ.	18 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic microminiature envelope with source and substrate interconnected, intended for u.h.f. and v.h.f. applications, such as u.h.f./v.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

This device is especially intended for use in pre-amplifiers in CATV tuners with a great tuning range up to 500 MHz.

QUICK REFERENCE DATA

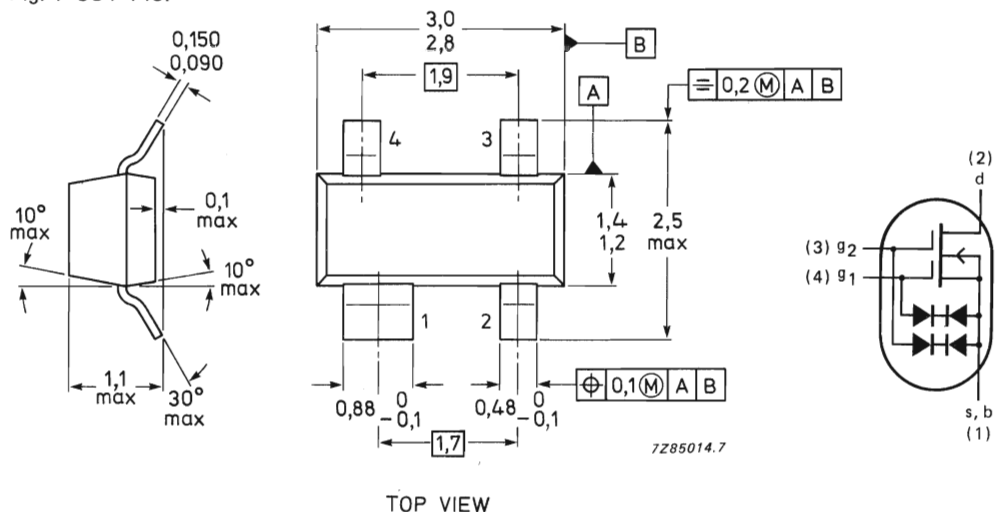
Drain-source voltage	V_{DS}	max.	20 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Total power dissipation up to $T_{amb} = 25^{\circ}\text{C}$	P_{tot}	max.	300 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ y_{fs} $	typ.	18 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	25 fF
Noise figure at $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$ $I_D = 10\text{ mA}$; $V_{DS} = 15\text{ V}$; $+V_{G2-S} = 4\text{ V}$; $f = 200\text{ MHz}$	F	typ.	1,0 dB

MECHANICAL DATA

Dimensions in mm

Marking code:
M83

Fig. 1 SOT-143.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (average)	$I_{D(AV)}$	max.	30 mA
Gate 1 source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	300 mW
Storage temperature	T_{stg}		-65 to $+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	$150\text{ }^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j-a}$	=	430 K/W
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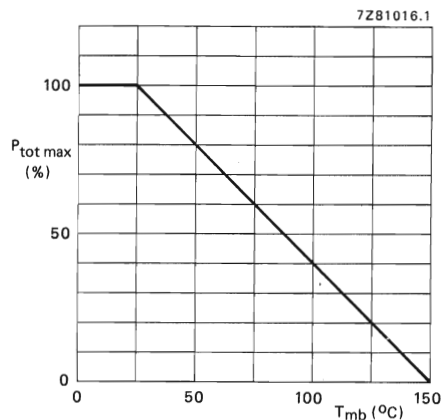


Fig. 2 Power derating curve.

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

STATIC CHARACTERISTICS

 $T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

gate 1;

 $\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$ $\pm I_{G1-SS} < 50\text{ nA}$

gate 2;

 $\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$ $\pm I_{G2-SS} < 50\text{ nA}$

Gate-source breakdown voltages

gate 1;

 $\pm I_{G1-SS} = 10\text{ mA}; V_{G2-S} = V_{DS} = 0$ $\pm V_{(BR)G1-SS} 6\text{ to }20\text{ V}$

gate 2;

 $\pm I_{G2-SS} = 10\text{ mA}; V_{G1-S} = V_{DS} = 0$ $\pm V_{(BR)G2-SS} 6\text{ to }20\text{ V}$

Gate-source cut-off voltages

gate 1;

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}$ $-V_{(P)G1-S} < 2,5\text{ V}$

gate 2;

 $I_D = 20\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; V_{G1-S} = 0$ $-V_{(P)G2-S} < 2,0\text{ V}$

Drain-source cut-off voltage

 $V_{DS} = 15\text{ V}; V_{G2-S} = 4\text{ V}; V_{G1-S} = 0$ $I_{DSS} 2\text{ to }20\text{ mA}$

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10\text{ mA}; V_{DS} = 15\text{ V}; +V_{G2-S} = 4\text{ V}; T_{amb} = 25^{\circ}\text{C}$ Transfer admittance at $f = 1\text{ kHz}$ $|y_{fs}| > 15\text{ mS}$
typ. 18 mSInput capacitance at gate 1; $f = 1\text{ MHz}$ C_{ig1-s} typ. 2,5 pFInput capacitance at gate 2; $f = 1\text{ MHz}$ C_{ig2-s} typ. 1,2 pFFeedback capacitance at $f = 1\text{ MHz}$ C_{rs} typ. 25 fFOutput capacitance at $f = 1\text{ MHz}$ C_{os} typ. 1,0 pFNoise figure at $f = 200\text{ MHz}; G_S = 2\text{ mS}; B_S = B_S\text{ opt}$ F typ. 1,0 dB ←Power gain at $G_S = 2\text{ mS}; B_S = B_S\text{ opt}$ $G_L = 0,5\text{ mS}; B_L = B_L\text{ opt}; f = 200\text{ MHz}$ G_p typ. 25 dB ←

DEVELOPMENT DATA

SILICON N-CHANNEL DUAL IG-MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with source and substrate connected to the case, intended for a wide range of v.h.f. applications, such as v.h.f. television tuners, f.m. tuners, as well as for applications in communication, instrumentation and control.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

The tetrode configuration, a series arrangement of two gate controlled channels, offers:

- a) very low feedback capacitance providing the possibility of more than 40 dB gain control in r.f. amplifiers requiring negligible a.g.c. power.
- b) excellent signal handling capability over the entire gain control range.
- c) low noise figure combined with high gain.

QUICK REFERENCE DATA

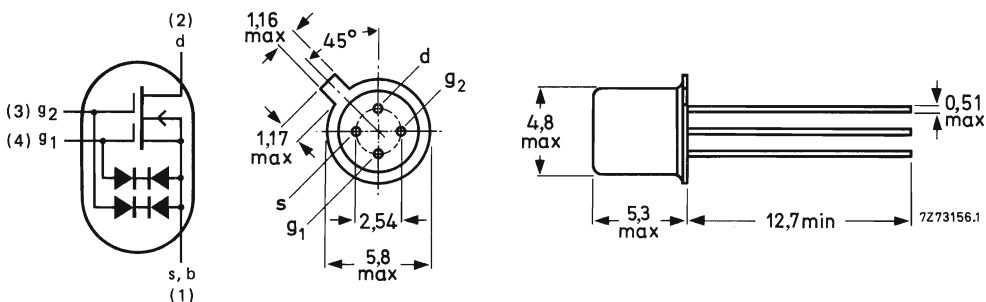
Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	50 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300 mW
Junction temperature	T_j	max.	175 $^{\circ}\text{C}$
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	$ Y_{fs} $	typ.	15 mS
Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 10\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$	C_{rs}	typ.	30 fF
Noise figure at optimum source admittance $I_D = 10\text{ mA}$; $V_{DS} = 10\text{ V}$; $+V_{G2-S} = 4\text{ V}$ $G_S = 1,2\text{ mS}$; $-B_S = 5,7\text{ mS}$; $f = 200\text{ MHz}$	F	typ.	2,3 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.

Source and substrate connected to the case.



Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d. c. or average)	I_D	max.	50	mA
Drain current (peak value)	I_{DM}	max.	100	mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	300	mW
Storage temperature	T_{stg}	-65 to +175	$^{\circ}\text{C}$	
Junction temperature	T_j	max.	175	$^{\circ}\text{C}$
THERMAL RESISTANCE				
From junction to ambient in free air	$R_{th\ j-a}$	=	500	K/W

STATIC CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off currents

$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	10	nA
$\pm V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0; T_j = 150\text{ }^{\circ}\text{C}$	$\pm I_{G1-SS}$	<	10	μA
$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	10	nA
$\pm V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0; T_j = 150\text{ }^{\circ}\text{C}$	$\pm I_{G2-SS}$	<	10	μA

Gate-source breakdown voltages

$\pm I_{G1-SS} = 0,1\text{ mA}; V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	6,0 to 20	V
$\pm I_{G2-SS} = 0,1\text{ mA}; V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	6,0 to 20	V

Drain current

$V_{DS} = 10\text{ V}; V_{G1-S} = 0; +V_{G2-S} = 4\text{ V}$	I_{DSS}	20 to 55	mA ¹⁾
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Gate 1-source voltage

$I_D = 10\text{ mA}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{G1-S}$	0,6 to 2,1	V
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Gate-source cut-off voltages

$I_D = 10\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; +V_{G2-S} = 4\text{ V}$	$-V_{(P)G1-S}$	1,5 to 3,8	V
$I_D = 10\text{ }\mu\text{A}; V_{DS} = 10\text{ V}; V_{G1-S} = 0$	$-V_{(P)G2-S}$	1,5 to 3,4	V

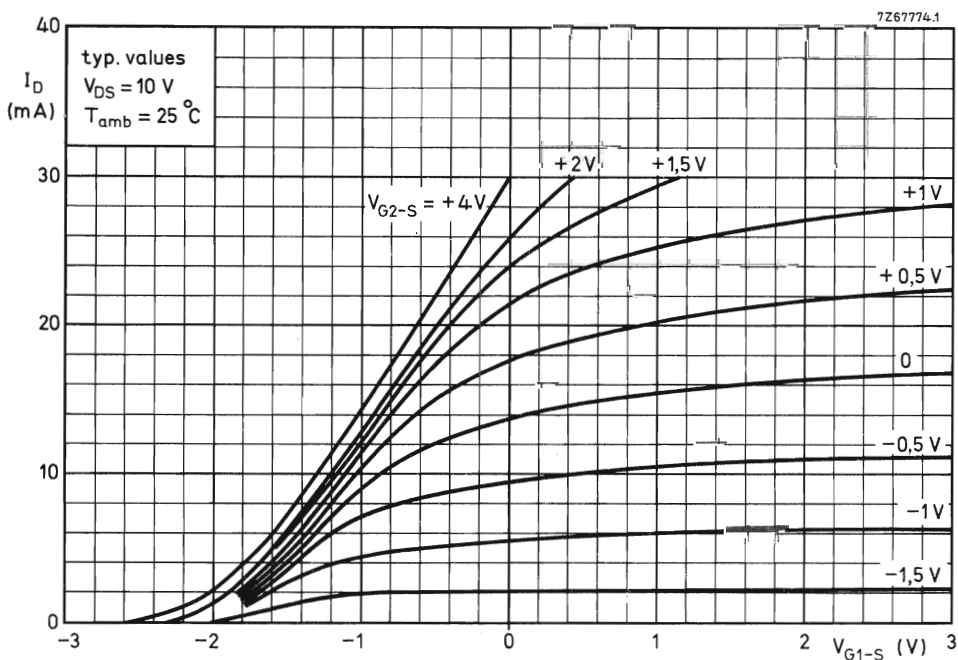
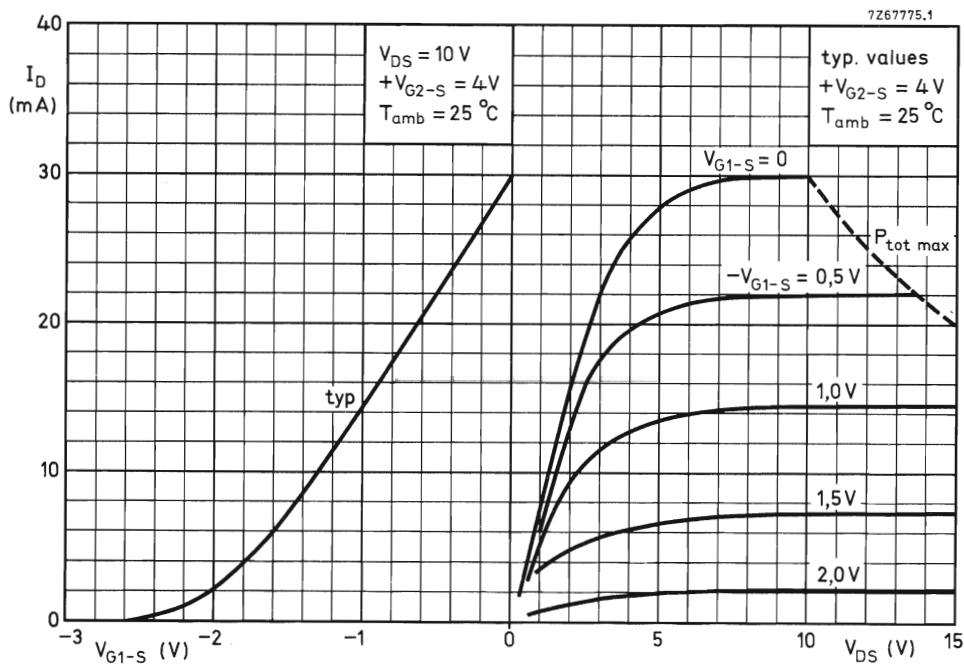
¹⁾ Measured under pulse conditions.

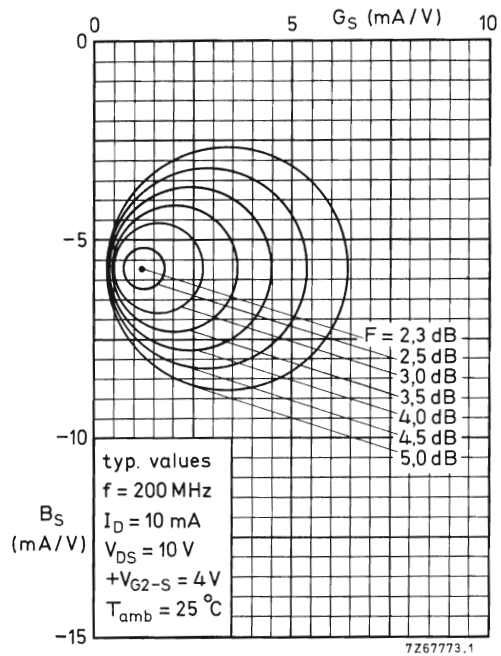
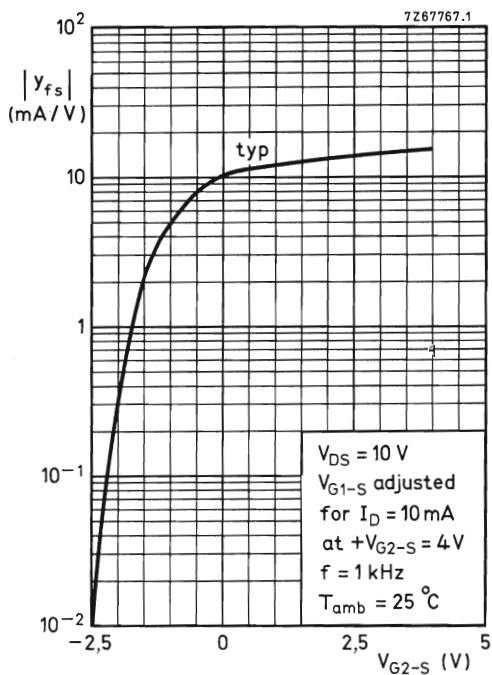
DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10 \text{ mA}$; $V_{DS} = 10 \text{ V}$; $+V_{G2-S} = 4 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$

Transfer admittance at $f = 1 \text{ kHz}$	$ y_{fs} $	$>$ typ.	12 15	mS mS
Input capacitance at $f = 1 \text{ MHz}$	C_{is}	typ.	5,5	pF
Feedback capacitance at $f = 1 \text{ MHz}$	C_{rs}	typ.	30	fF
Output capacitance at $f = 1 \text{ MHz}$	C_{os}	typ.	3,5	pF
Noise figure at optimum source admittance				
$G_S = 0,95 \text{ mS}$; $-B_S = 5,0 \text{ mS}$; $f = 100 \text{ MHz}$	F	typ.	1,9	dB
$G_S = 1,20 \text{ mS}$; $-B_S = 5,7 \text{ mS}$; $f = 200 \text{ MHz}$	F	typ. <	2,3 3,0	dB dB
Cross modulation at $f = 200 \text{ MHz}$				
Wanted signal at $f_o = 197,5 \text{ MHz}$				
Unwanted signal at $f_{int} = 202,5 \text{ MHz}$				
Interference voltage at g_1 for $K = 1\%$	V_{int}	typ.	100	mV ¹⁾

1) Cross modulation is defined here as the voltage at g_1 of an unwanted signal with 80% modulation depth, giving 0,8% modulation depth on the wanted signal (a. m. definition).





circles of constant noise figure

DEVICE DATA

VERTICAL DMOS-FETS

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use as line current interruptor in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

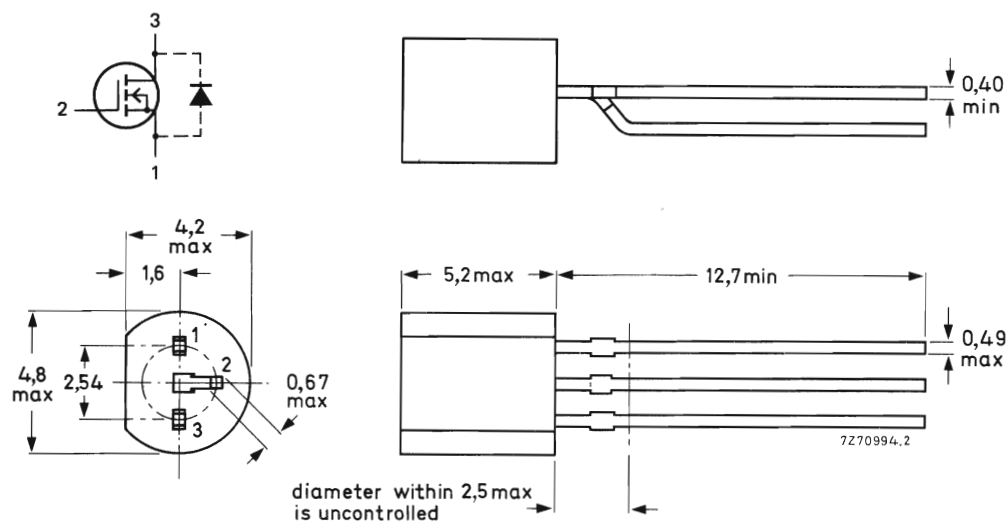
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage	V_{GS}	max.	15 V
Drain current (d.c.)	I_D	max.	120 mA
Total power dissipation up to $T_C = 25^\circ\text{C}$	P_{tot}	max.	500 mW
Junction temperature	T_j	max.	150°C
Drain-source ON-resistance $V_{GS} = 2,6\text{ V}; I_D = 20\text{ mA}$	R_{DSon}	max.	$28\ \Omega$

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Drain-gate voltage	V_{DGS}	max.	200 V
Gate-source voltage	V_{GS}	max.	15 V
Drain current (d.c.)	I_D	max.	120 mA
Total power dissipation up to $T_C = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	500 mW
Storage temperature	T_{stg}		-55 to +150 $^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	150 K/W
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CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Drain-source breakdown voltage

 $V_{GS} = 0; I_D = 100\text{ }\mu\text{A}$

$V_{(BR)DS}$	>	200 V
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Gate-source leakage current

 $V_{GS} = 15\text{ V}; V_{DS} = 0$

I_{GSoff}	<	10 nA
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Drain cut-off current

 $V_{DS} = 130\text{ V}; V_{GS} = 0$

I_{DSS}	<	30 nA
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 $V_{DS} = 70\text{ V}; V_{GS} = 0,2\text{ V}$

I_{DSX}	<	1 μA
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Drain-source ON-resistance

 $V_{GS} = 2,6\text{ V}; I_D = 20\text{ mA}$

R_{DSon}	typ.	15 Ω
	<	28 Ω

 $V_{GS} = 10\text{ V}; I_D = 250\text{ mA}$

R_{DSon}	typ.	6 Ω
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Gate threshold voltage

 $I_D = 1\text{ mA}; V_{DS} = V_{GS}$

$V_{GS(th)}$	>	0,8 V
	typ.	1,8 V
	<	2,8 V

Transfer admittance at $f = 1\text{ kHz}$ $I_D = 250\text{ mA}; V_{DS} = 15\text{ V}$

$ y_{fs} $	typ.	250 mS
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Input capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$

C_{is}	typ.	70 pF
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Output capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$

C_{os}	typ.	20 pF
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Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$

C_{rs}	typ.	5 pF
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Switching times (see Figs 2 and 3)

 $I_D = 250\text{ mA}; V_{DS} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$

t_{on}	typ.	4 ns
	<	10 ns
t_{off}	typ.	15 ns
	<	25 ns

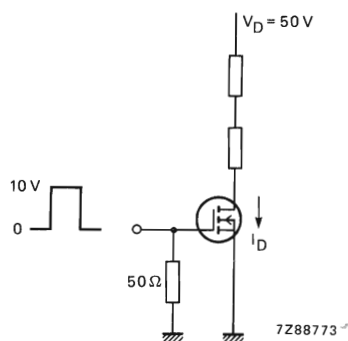


Fig. 2 Switching times test circuit.

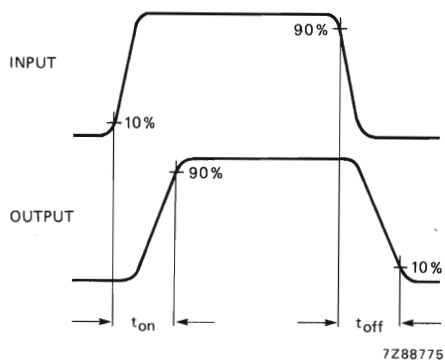


Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon} .
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

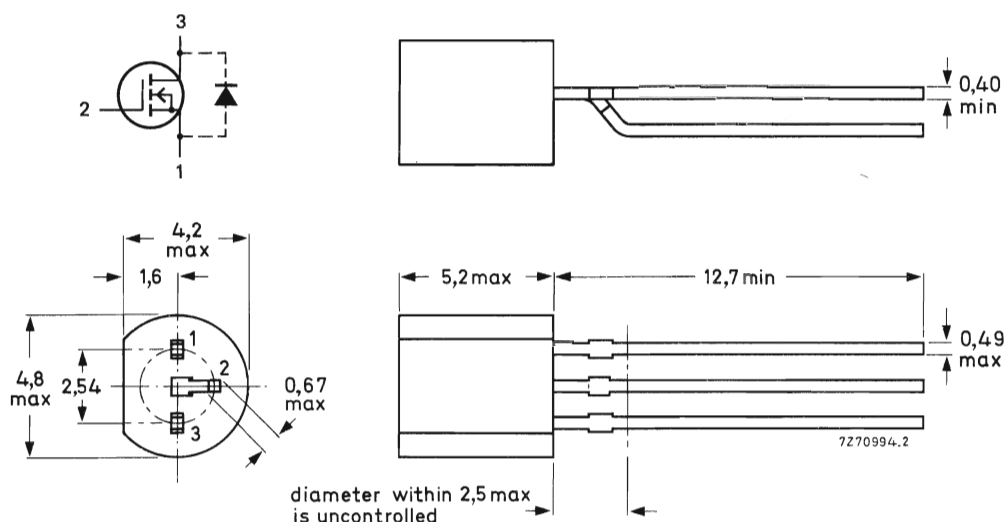
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60 V
Gate-source voltage	V_{GS}	max.	15 V
Drain current (d.c.)	I_D	max.	500 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	830 mW
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$
Drain-source ON-resistance $V_{GS} = 10\text{ V}; I_D = 200\text{ mA}$	R_{DSon}	max.	5 Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	60 V
Drain-gate voltage	V_{DG}	max.	60 V
Gate-source voltage	V_{GS}	max.	15 V
Drain current (d.c.) at $T_c = 25\text{ }^{\circ}\text{C}$	I_D	max.	500 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	830 mW
Storage temperature	T_{stg}		-55 to +150 $^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	150 K/W
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CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Drain-source breakdown voltage

$V_{GS} = 0; I_D = 100\text{ }\mu\text{A}$	$V_{(BR)DS}$	>	60 V
		typ.	90 V

Gate threshold voltage

$V_{GS} = V_{DS}; I_D = 1\text{ mA}$	$V_{GS(th)}$	>	0,8 V
		<	3,0 V

Gate-source leakage current

$V_{GS} = 15\text{ V}; V_{DS} = 0$	I_{GSoff}	<	10 nA
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Drain cut-off current

$V_{DS} = 25\text{ V}; V_{GS} = 0$	I_{DSS}	<	0,5 μA
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Drain-source ON-resistance *

$V_{GS} = 10\text{ V}; I_D = 200\text{ mA}$	R_{DSon}	typ.	2,5 Ω
		<	5,0 Ω

Forward transconductance *

$V_{DS} = 10\text{ V}; I_D = 200\text{ mA};$ $f = 1\text{ kHz}$	g_{fs}	typ.	200 mS
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Capacitances at $f = 1\text{ MHz}$

$V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{iss}	typ.	25 pF
		<	40 pF

	C_{os}	typ.	22 pF
		<	30 pF

	C_{rs}	typ.	6 pF
		<	10 pF

Switching times at $I_D = 200\text{ mA}$

$I_D = 200\text{ mA}; V_{DS} = 50\text{ V};$ $V_{GS} = 0\text{ to }10\text{ V}$	t_{on}	typ.	4 ns
		<	10 ns
	t_{off}	typ.	4 ns
		<	10 ns

* $t_p = 80\text{ }\mu\text{s}; \delta = 0,01.$

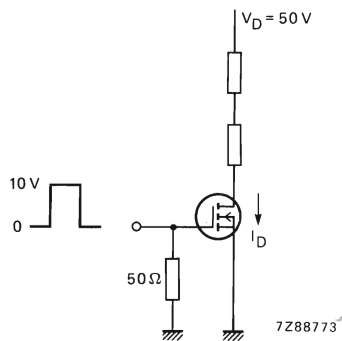


Fig. 2 Switching times test circuit

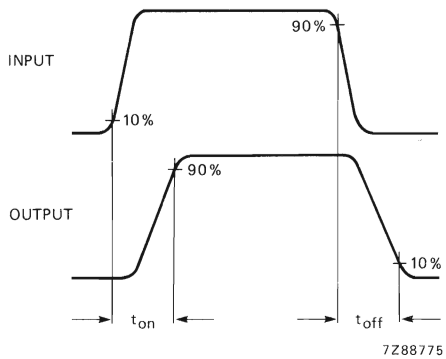


Fig. 3 Input and output waveforms

P-CHANNEL VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

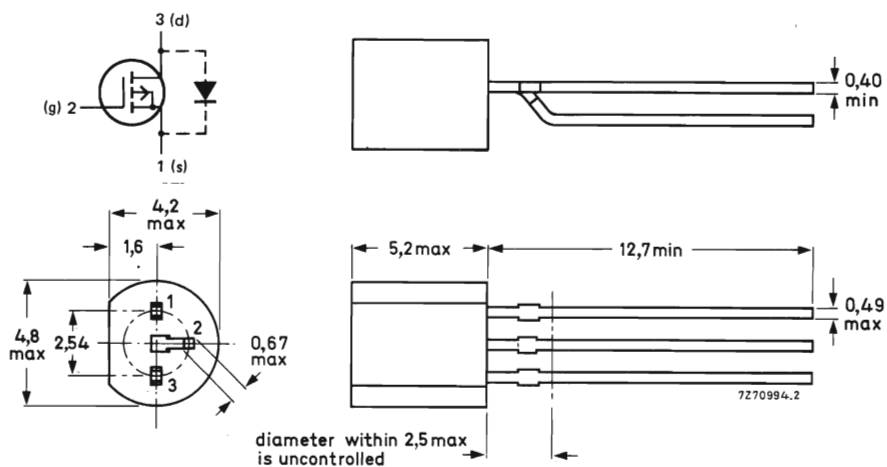
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	45 V
Gate-source voltage (open drain)	$-V_{GS0}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,25 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	0,83 W
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	R_{DSon}	typ. <	9 Ω 14 Ω
Transfer admittance at $f = 1\text{ kHz}$ $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	125 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	45 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,25 A
Drain current (peak value)	$-I_{DM}$	max.	0,5 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	0,83 W
Storage temperature	T_{stg}		-65 to $+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$	=	150 K/W
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CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Drain-source breakdown voltage $-I_D = 100\text{ }\mu\text{A}; V_{GS} = 0$	$-V_{(BR)DS}$	min.	45 V
Drain-source leakage current $-V_{DS} = 25\text{ V}; V_{GS} = 0$	$-I_{DSS}$	max.	0,5 μA
Gate-source leakage current $-V_{GS} = 15\text{ V}; V_{DS} = 0$	$-I_{GSS}$	max.	20 nA
Gate threshold voltage $-I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$-V_{GS(th)}$	min. max.	1,0 V 3,5 V
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	R_{DSon}	typ. max.	9 Ω 14 Ω
Transfer admittance at $f = 1\text{ kHz}$ $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	125 mS
Input capacitance at $f = 1\text{ MHz}$ → $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{is}	typ. <	30 pF 45 pF
Output capacitance at $f = 1\text{ MHz}$ → $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{os}	typ. <	20 pF 30 pF
Feedback capacitance at $f = 1\text{ MHz}$ → $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{rs}	typ. <	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D = 200\text{ mA}; -V_D = 40\text{ V}; -V_{GS} = 0$ to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

* Transistor mounted on printed-circuit board, max. lead length 4 mm.

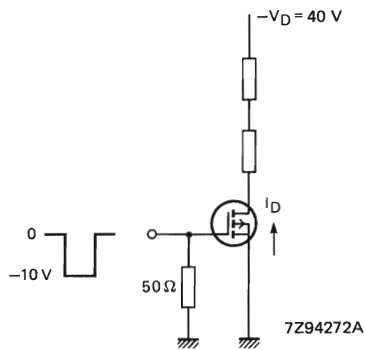


Fig. 2 Switching times test circuit.

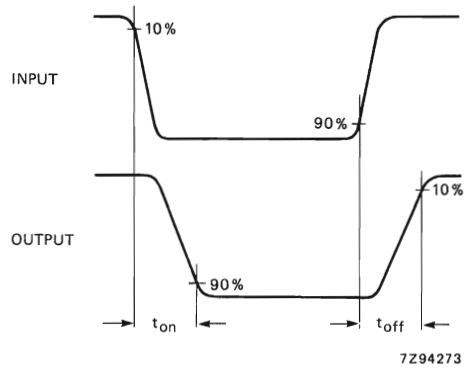


Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

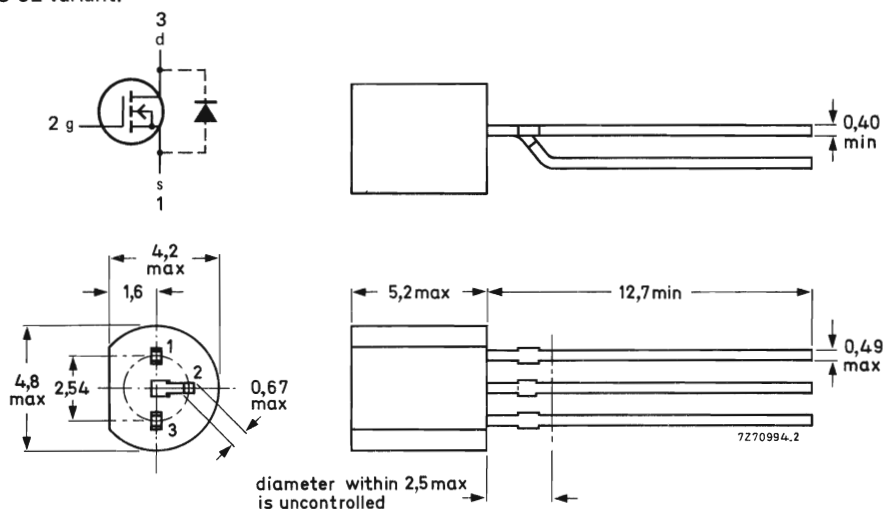
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,5 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	1 W
Drain-source ON-resistance $I_D = 500\text{ mA}$; $V_{GS} = 10\text{ V}$	R_{DSon}	typ. max.	2 Ω 4 Ω
Transfer admittance $I_D = 500\text{ mA}$; $V_{DS} = 15\text{ V}$; $f = 1\text{ kHz}$	$ y_{fs} $	typ.	300 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	V_{GS0}	max.	20 V
Drain current (d.c.)	I_D	max.	0,5 A
Drain current (peak)	I_{DM}	max.	1,0 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	1 W
Storage temperature	T_{stg}		$-65\text{ to }+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$	125 K/W
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CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Drain-source breakdown voltage

$I_D = 100\text{ }\mu\text{A}; V_{GS} = 0$

$V_{(BR)DS}$	>	80 V
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Drain-source leakage current

$V_{DS} = 60\text{ V}; V_{GS} = 0$

I_{DSS}	<	10 μA
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Gate-source leakage current

$V_{GS} = 20\text{ V}; V_{DS} = 0$

I_{GSS}	<	100 nA
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Gate threshold voltage

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

$V_{GS(th)}$	>	1,5 V
	<	3,5 V

Drain-source ON-resistance (see Fig. 4)

$I_D = 500\text{ mA}; V_{GS} = 10\text{ V}$

R_{DSon}	typ.	2,0 Ω
	<	4,0 Ω

Transfer admittance at $f = 1\text{ kHz}$

$I_D = 500\text{ mA}; V_{DS} = 15\text{ V}$

$ y_{fs} $	typ.	300 mS
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Input capacitance at $f = 1\text{ MHz}$

→ $V_{DS} = 10\text{ V}; V_{GS} = 0$

C_{is}	typ.	45 pF
	<	60 pF

Output capacitance at $f = 1\text{ MHz}$

→ $V_{DS} = 10\text{ V}; V_{GS} = 0$

C_{os}	typ.	30 pF
	<	45 pF

Feedback capacitance at $f = 1\text{ MHz}$

→ $V_{DS} = 10\text{ V}; V_{GS} = 0$

C_{rs}	typ.	8 pF
	<	12 pF

Switching times (see Figs 2 and 3)

$I_D = 500\text{ mA}; V_{DS} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$

t_{on}	<	10 ns
t_{off}	<	15 ns

* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

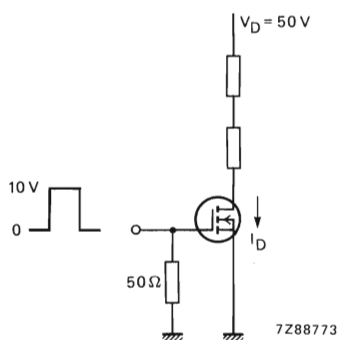


Fig. 2 Switching times test circuit.

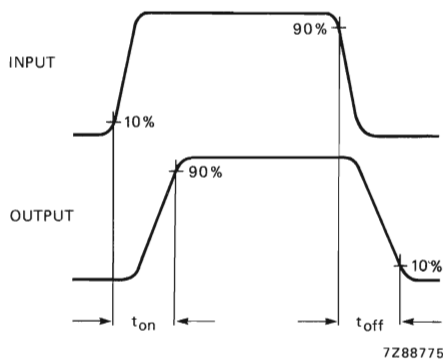


Fig. 3 Input and output waveforms.

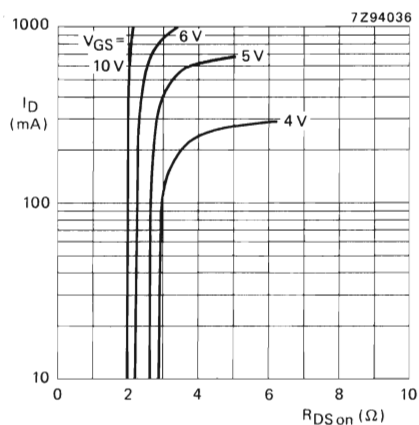
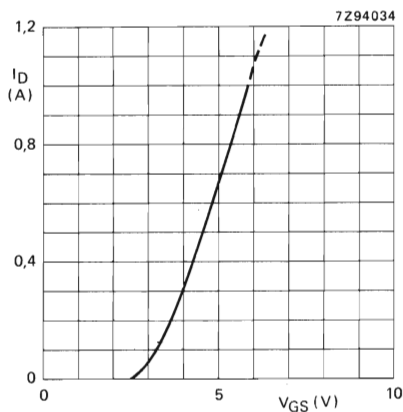
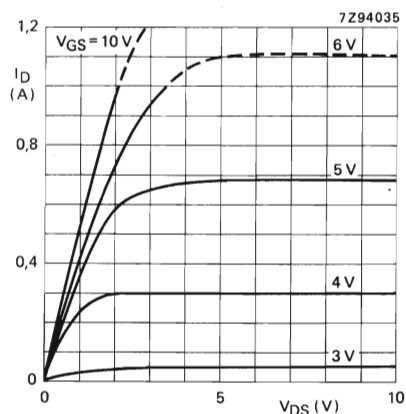
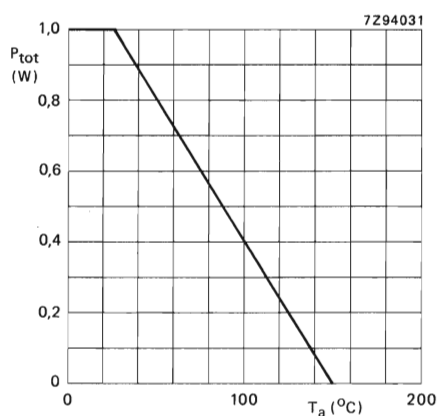
Fig. 4 $T_j = 25^\circ\text{C}$; typical values.Fig. 5 $T_j = 25^\circ\text{C}$; typical values at $V_{DS} = 10\text{ V}$.Fig. 6 $T_j = 25^\circ\text{C}$; typical values.

Fig. 7 Power derating curve.

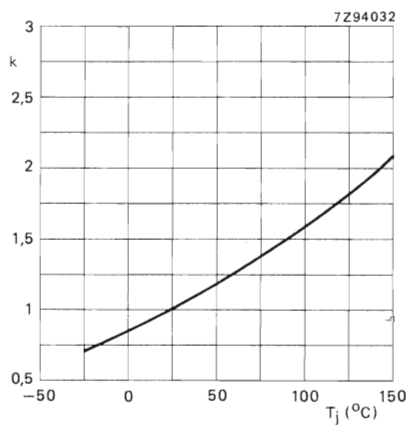


Fig. 8 $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^\circ C}}$; typ. values at 500 mA/10 V.

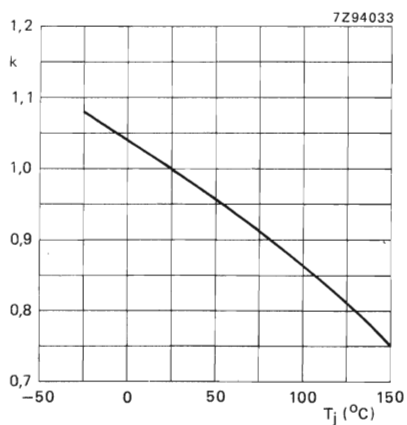


Fig. 9 $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^\circ C}}$; $V_{GS(th)}$ at 1 mA; typical values.

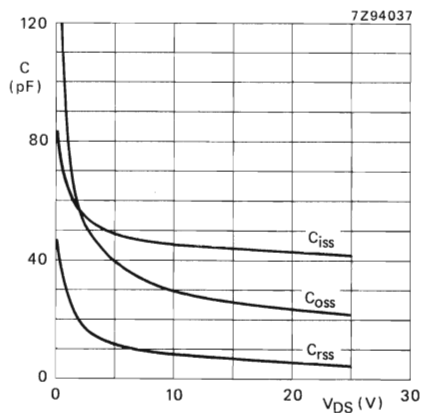


Fig. 10 $T_j = 25\ ^\circ C$; $V_{GS} = 0$; $f = 1\ MHz$; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

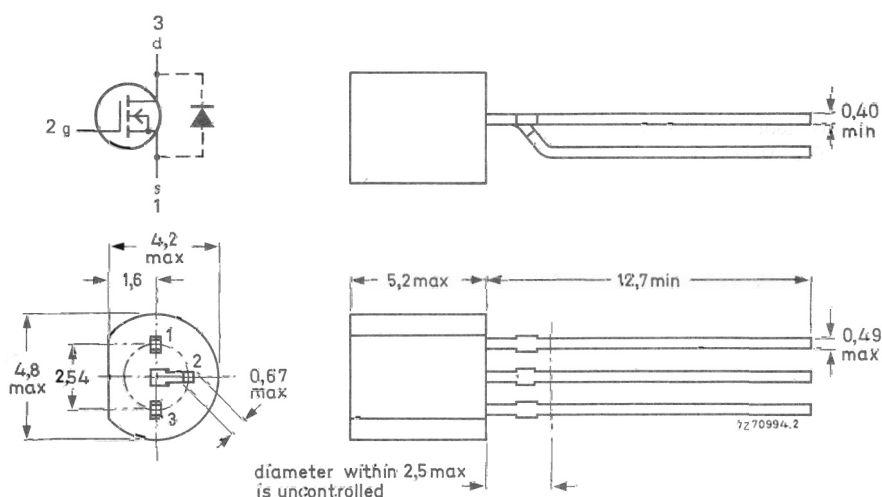
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	300 mA
Total power dissipation up to $T_{amb} = 25^\circ\text{C}$	P_{tot}	max.	0,83 W
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	$R_{DS(on)}$	typ. max.	7 Ω 10 Ω
Transfer admittance $I_D = 200$ mA; $V_{DS} = 5$ V; $f = 1$ kHz	$ y_{fs} $	typ.	150 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



Note: Various pinning are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	600 mA
Total power dissipation up to $T_{amb} = 25$ °C*	P_{tot}	max.	0,83 W
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$	150 K/W
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CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified

Drain-source breakdown voltage $I_D = 100$ μ A; $V_{GS} = 0$	$V_{(BR)DS}$	>	80 V
Drain-source leakage current $V_{DS} = 60$ V; $V_{GS} = 0$	I_{DSS}	<	1,0 μ A
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	<	100 nA
Gate threshold voltage $I_D = 1$ mA; $V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	1,5 V 3,5 V
Drain-source ON-resistance (see Fig. 4) $I_D = 150$ mA; $V_{GS} = 5$ V	R_{DSon}	typ. <	7 Ω 10 Ω
Transfer admittance at $f = 1$ kHz $I_D = 200$ mA; $V_{DS} = 5$ V	$ y_{fs} $	typ.	150 mS
Input capacitance at $f = 1$ MHz → $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ. <	15 pF 30 pF
Output capacitance at $f = 1$ MHz → $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ. <	13 pF 20 pF
Feedback capacitance at $f = 1$ MHz → $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ. <	3 pF 6 pF
Switching times (see Figs 2 and 3) $I_D = 200$ mA; $V_{DS} = 50$ V; $V_{GS} = 0$ to 10 V	t_{on}	typ. <	4 ns 10 ns
	t_{off}	typ. <	4 ns 10 ns

* Transistor mounted on printed circuit board, max. lead length 4 mm.

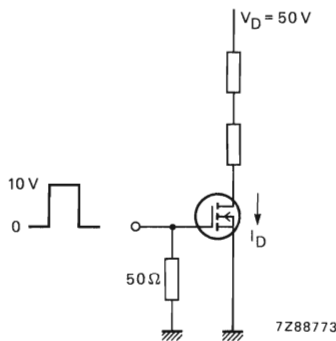


Fig. 2 Switching times test circuit.

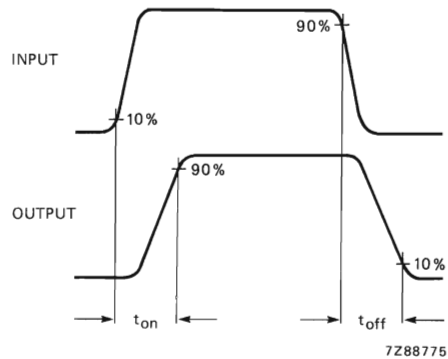


Fig. 3 Input and output waveforms.

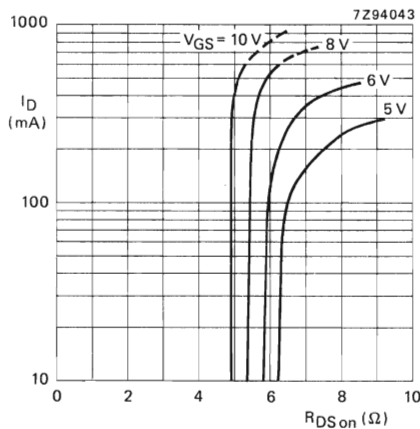


Fig. 4 $T_j = 25\text{ }^{\circ}\text{C}$; typical values.

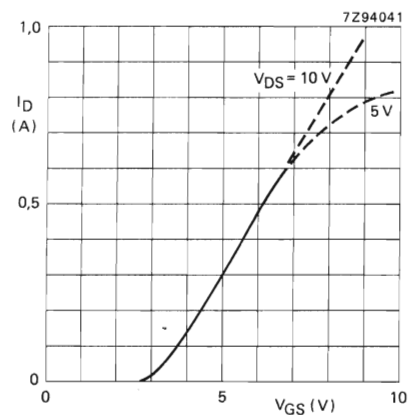


Fig. 5 $T_j = 25\text{ }^{\circ}\text{C}$; typical values.

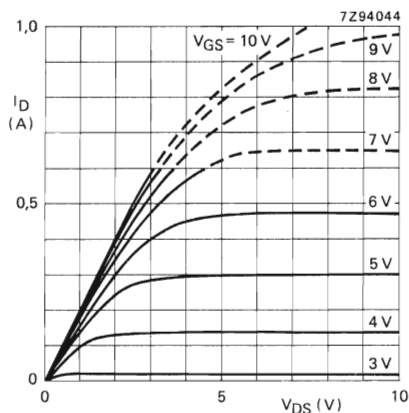


Fig. 6 $T_j = 25\text{ }^{\circ}\text{C}$; typical values.

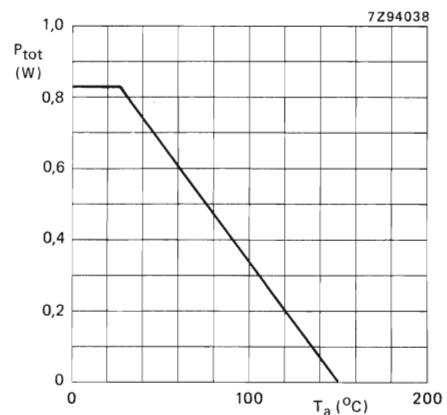


Fig. 7 Power derating curve.

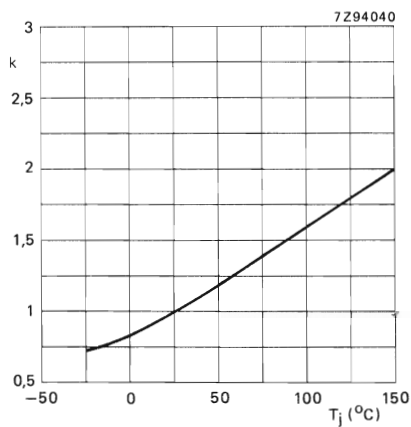


Fig. 8 $k = \frac{R_{DS \text{ on at } T_j}}{R_{DS \text{ on at } 25^\circ\text{C}}}$; typ. values at 150 mA/5 V.

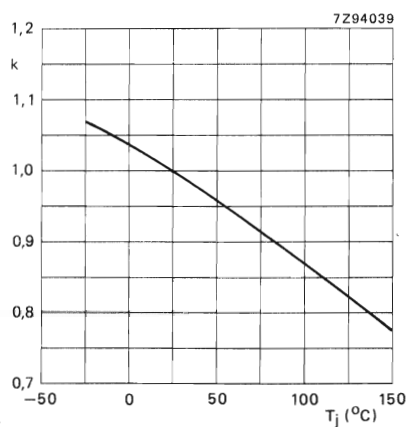


Fig. 9 $k = \frac{V_{GS(th) \text{ at } T_j}}{V_{GS(th) \text{ at } 25^\circ\text{C}}}$; $V_{GS(th)}$ at 1 mA; typical values.

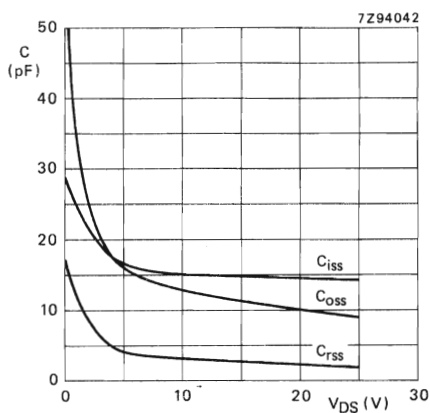


Fig. 10 $T_j = 25^\circ\text{C}$; $V_{GS} = 0$; $f = 1 \text{ MHz}$; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

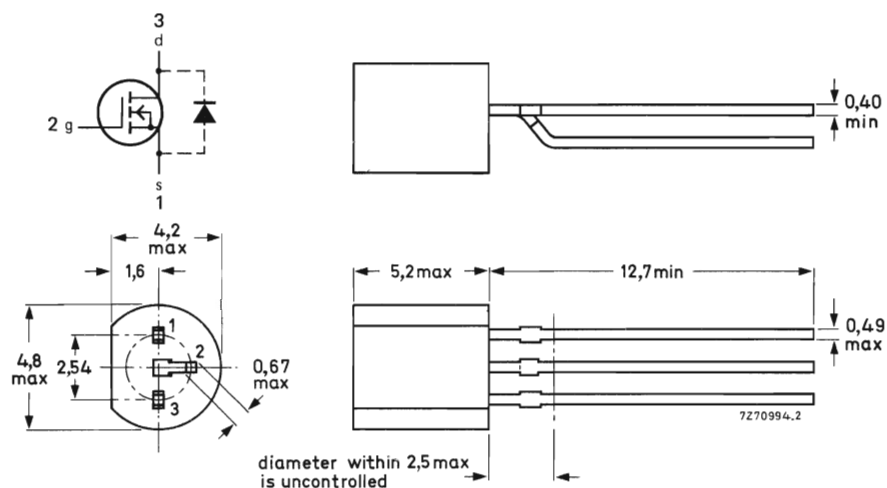
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	250 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	1 W
Drain-source ON-resistance $I_D = 250\text{ mA}$; $V_{GS} = 10\text{ V}$	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance $I_D = 250\text{ mA}$; $V_{DS} = 15\text{ V}$; $f = 1\text{ kHz}$	$ y_{fs} $	typ.	250 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



Note: Various pinning are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	1 W
Storage temperature	T_{stg}		-65 to $+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	$150\text{ }^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$		125 K/W
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CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Drain-source breakdown voltage

$I_D = 100\text{ }\mu\text{A}; V_{GS} = 0$

$V_{(BR)DS} > 200\text{ V}$

Drain-source leakage current

$V_{DS} = 160\text{ V}; V_{GS} = 0$

$I_{DSS} < 10\text{ }\mu\text{A}$

Gate-source leakage current

$V_{GS} = 20\text{ V}; V_{DS} = 0$

$I_{GSS} < 100\text{ nA}$

Gate threshold voltage

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

$V_{GS(th)} > 0,8\text{ V}$
 $< 2,8\text{ V}$

Drain-source ON-resistance (see Fig. 4)

$I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$

R_{DSon} typ. $6\text{ }\Omega$
 $< 12\text{ }\Omega$

Transfer admittance at $f = 1\text{ kHz}$

$I_D = 250\text{ mA}; V_{DS} = 15\text{ V}$

$|y_{fs}|$ typ. 250 mS

Input capacitance at $f = 1\text{ MHz}$

$V_{DS} = 10\text{ V}; V_{GS} = 0$

C_{is} typ. 70 pF
 $< 90\text{ pF}$

Output capacitance at $f = 1\text{ MHz}$

$V_{DS} = 10\text{ V}; V_{GS} = 0$

C_{os} typ. 20 pF
 $< 30\text{ pF}$

Feedback capacitance at $f = 1\text{ MHz}$

$V_{DS} = 10\text{ V}; V_{GS} = 0$

C_{rs} typ. 5 pF
 $< 10\text{ pF}$

Switching times (see Figs 2 and 3)

$I_D = 250\text{ mA}; V_{DS} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$

t_{on} typ. 4 ns
 $< 10\text{ ns}$

t_{off} typ. 15 ns
 $< 25\text{ ns}$

* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

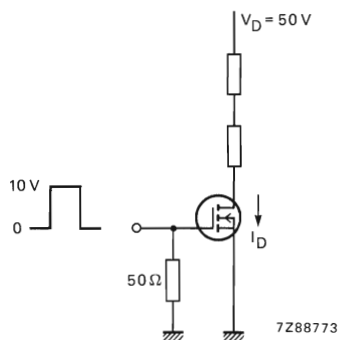


Fig. 2 Switching times test circuit.

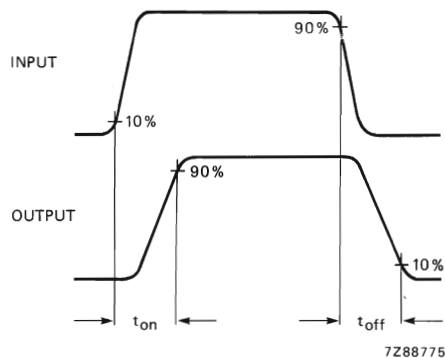


Fig. 3 Input and output waveforms.

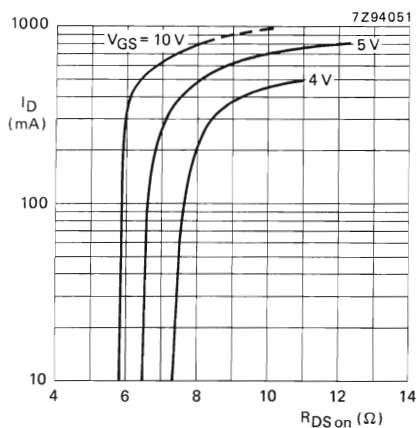
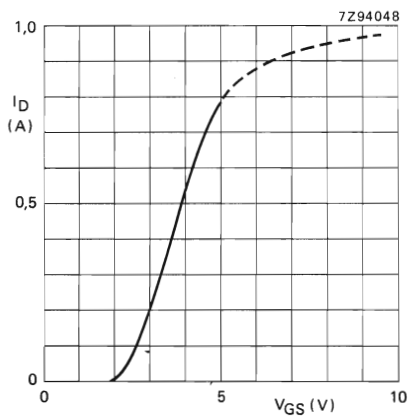
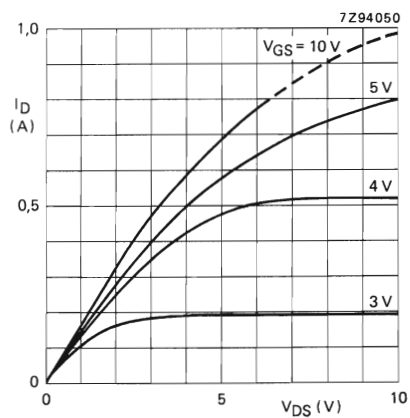
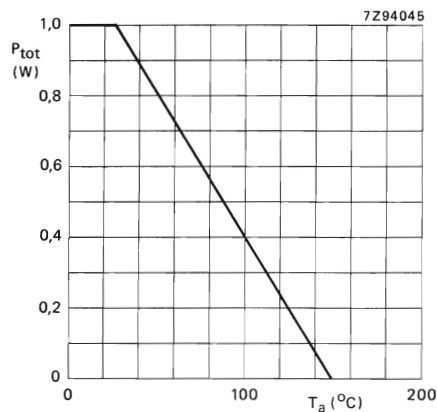
Fig. 4 $T_j = 25\text{ }^{\circ}\text{C}$; typical values.Fig. 5 $T_j = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 10\text{ V}$; typical values.Fig. 6 $T_j = 25\text{ }^{\circ}\text{C}$; typical values.

Fig. 7 Power derating curve.

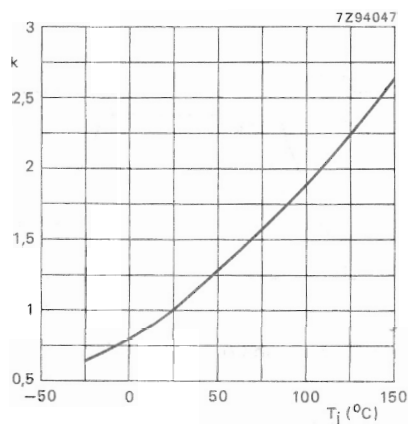


Fig. 8 $k = \frac{R_{DS \text{ on at } T_j}}{R_{DS \text{ on at } 25^\circ\text{C}}}$; at 400 mA/10 V; typical values.

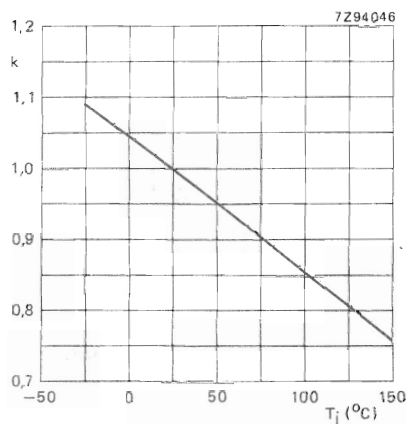


Fig. 9 $k = \frac{V_{GS(th) \text{ at } T_j}}{V_{GS(th) \text{ at } 25^\circ\text{C}}}$; $V_{GS(th)}$ at 1 mA; typical values.

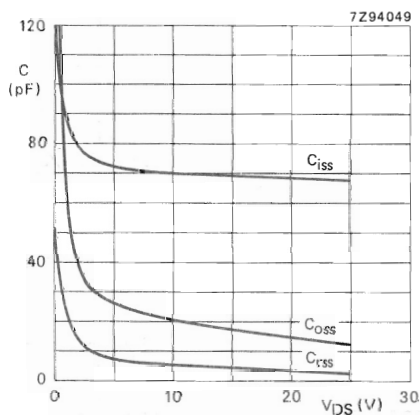


Fig. 10 $T_j = 25^\circ\text{C}$; $V_{GS} = 0$; $f = 1 \text{ MHz}$; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	300 mA
Total power dissipation up to $T_{amb} = 25^\circ C$	P_{tot}	max.	1 W
Drain-source ON-resistance $I_D = 15$ mA; $V_{GS} = 3$ V	$R_{DS(on)}$	typ. max.	7 Ω 10 Ω
Transfer admittance $I_D = 300$ mA; $V_{DS} = 15$ V; $f = 1$ kHz	$ y_{fs} $	typ.	250 mS

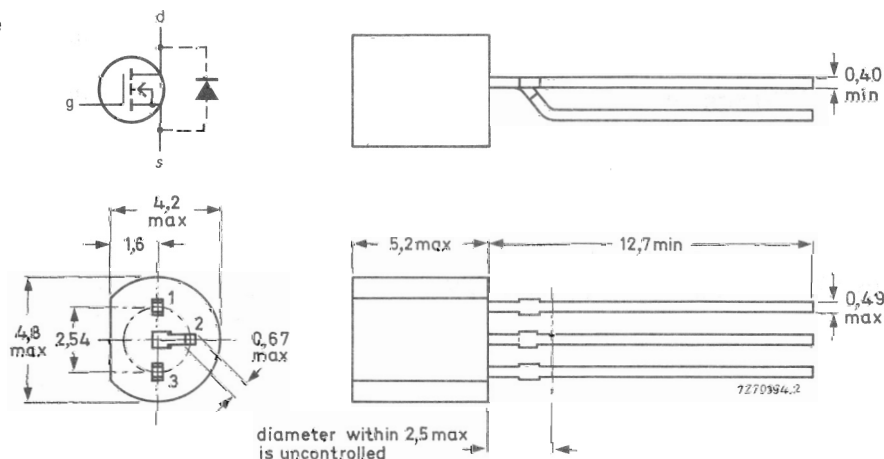
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

- 1 = source
2 = gate
3 = drain



Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to $T_{amb} = 25$ °C*	P_{tot}	max.	1 W
Storage temperature	T_{stg}		-65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient*	R_{thj-a}	125 K/W
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CHARACTERISTICS $T_j = 25$ °C unless otherwise specified

Drain-source breakdown voltage $I_D = 100$ μ A; $V_{GS} = 0$	$V_{(BR)DS}$	>	180 V
Drain-source leakage current $V_{DS} = 120$ V; $V_{GS} = 0$	I_{DSS}	<	10 μ A
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	<	100 nA
Gate threshold voltage $I_D = 100$ μ A; $V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	0,7 V 2,4 V
Drain-source ON-resistance (see Fig. 4) $I_D = 15$ mA; $V_{GS} = 3$ V	R_{DSon}	typ. <	7 Ω 10 Ω
$I_D = 300$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	6 Ω
Transfer admittance at $f = 1$ kHz $I_D = 300$ mA; $V_{DS} = 15$ V	$ y_{fs} $	typ.	250 mS
Input capacitance at $f = 1$ MHz → $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ. <	50 pF 65 pF
Output capacitance at $f = 1$ MHz → $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ. <	20 pF 30 pF
Feedback capacitance at $f = 1$ MHz → $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ. <	6 pF 10 pF
Switching times (see Figs 2 and 3) $I_D = 300$ mA; $V_{DS} = 50$ V; $V_{GS} = 0$ to 10 V	t_{on} t_{off}	< <	10 ns 15 ns

* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

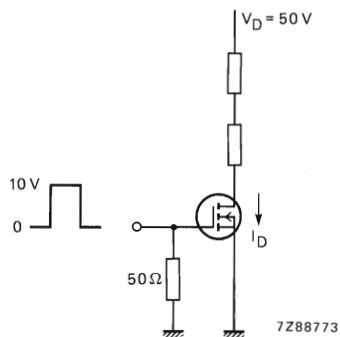


Fig. 2 Switching times test circuit.

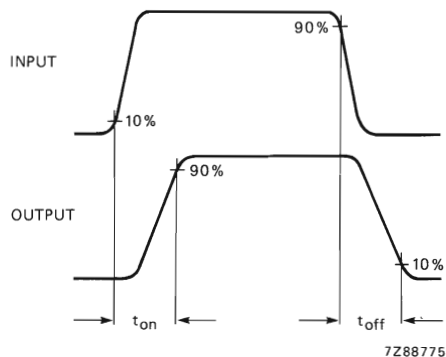


Fig. 3 Input and output waveforms.

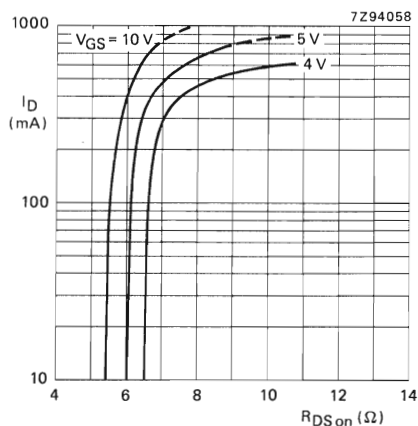
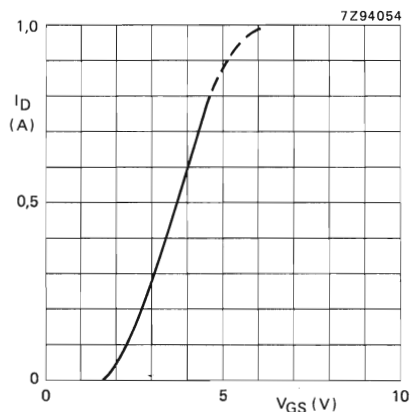
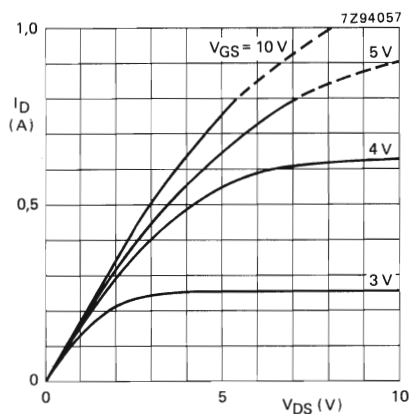
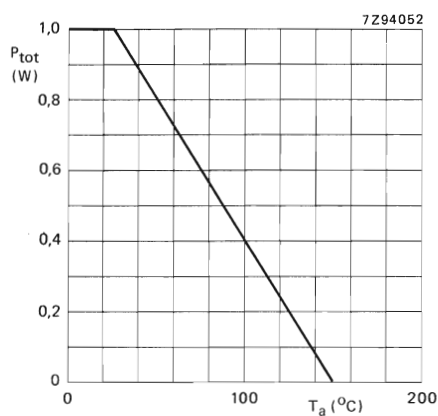
Fig. 4 $T_j = 25^\circ\text{C}$; typical values.Fig. 5 $T_j = 25^\circ\text{C}$; $V_{DS} = 10\text{ V}$; typ. values.Fig. 6 $T_j = 25^\circ\text{C}$; typical values.

Fig. 7 Power derating curve.

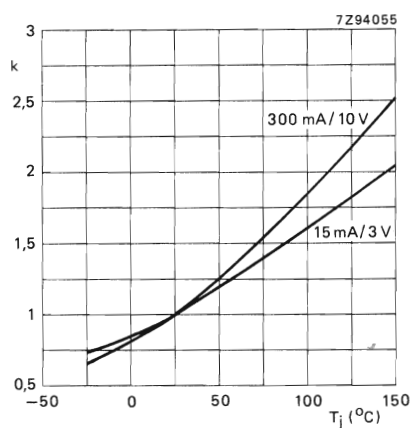


Fig. 8 $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^\circ C}}$; typical values.

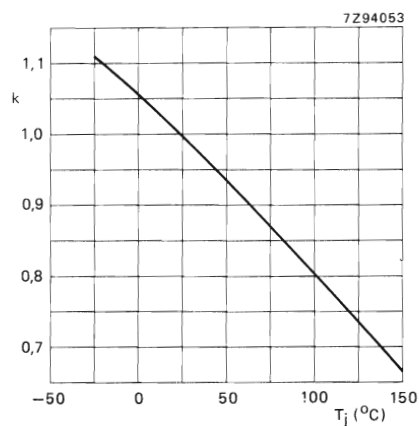


Fig. 9 $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^\circ C}}$; $V_{GS(th)}$ at 0,1 mA; typical values.

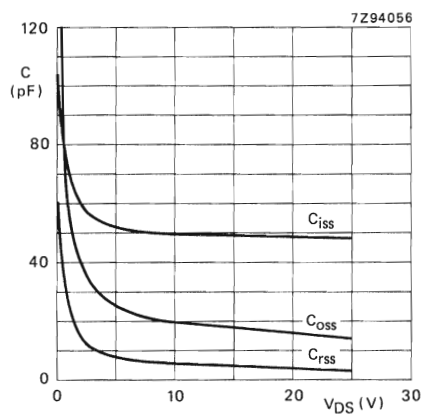


Fig. 10 $T_j = 25\ ^\circ C$; $V_{GS} = 0$; $f = 1\ MHz$; typical values.

HIGH-VOLTAGE N-CHANNEL VERTICAL D-MOS TRANSISTOR

High-voltage N-channel vertical D-MOS transistor in plastic TO-126 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching, low power switching losses
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	450 V
Drain-source voltage (non-repetitive peak; $t_p \leq 50 \mu s$)	$V_{DS(SM)}$	max.	525 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,75 A
Total power dissipation up to $T_{mb} = 75 ^\circ C$	P_{tot}	max.	15 W
Drain-source ON-resistance $I_D = 500 \text{ mA}; V_{GS} = 10 \text{ V}$	$R_{DS(on)}$	typ.	15 Ω
Transfer admittance $I_D = 250 \text{ mA}; V_{DS} = 20 \text{ V}; f = 1 \text{ kHz}$	$ y_{fs} $	typ.	400 mS

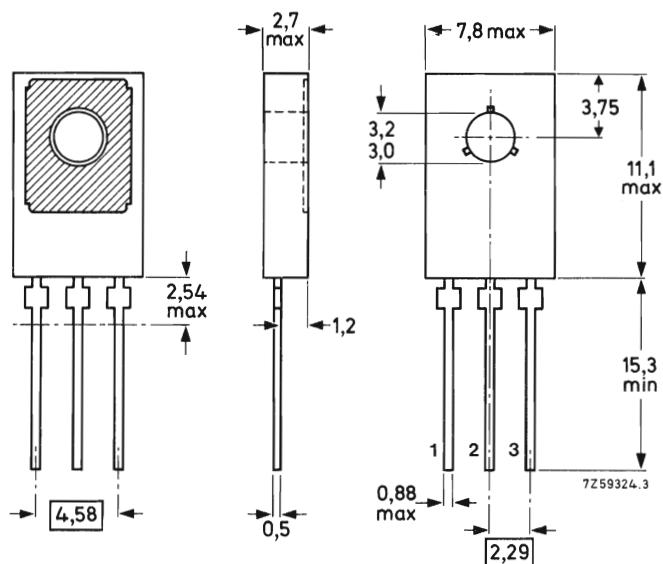
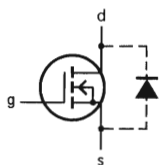
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-126.

Drain connected
to mounting base.

Pinning;
1 = source
2 = drain
3 = gate



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	450 V
Drain-source voltage (non-repetitive peak; $t_p \leq 50 \mu s$)	$V_{DS(SM)}$	max.	525 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,75 A
Drain current (peak)	I_{DM}	max.	1,5 A
Total power dissipation up to $T_{mb} = 75 ^\circ C$	P_{tot}	max.	15 W
Storage temperature	T_{stg}	-65 to +150	$^\circ C$
Junction temperature	T_j	max.	150 $^\circ C$

THERMAL RESISTANCE

From junction to ambient	$R_{th j-a}$	100 K/W
From junction to mounting base	$R_{th j-mb}$	5 K/W

CHARACTERISTICS

$T_j = 25 ^\circ C$ unless otherwise specified

Drain-source breakdown voltage $I_D = 100 \mu A$; $V_{GS} = 0$	$V_{(BR)DS}$	>	450 V
Drain-source leakage current $V_{DS} = 350 V$; $V_{GS} = 0$	I_{DSS}	<	25 μA
Gate-source leakage current $V_{GS} = 20 V$; $V_{DS} = 0$	I_{GSS}	<	100 nA
Gate-source cut-off voltage $I_D = 1 mA$; $V_{DS} = V_{GS}$	$V_{(P)GS}$	> <	2,0 V 4,0 V
Drain-source ON-resistance (see Fig. 4) $I_D = 100 mA$; $V_{GS} = 10 V$	R_{DSon}	typ. <	10 Ω 14 Ω
$I_D = 500 mA$; $V_{GS} = 10 V$	R_{DSon}	typ.	15 Ω
Transfer admittance at $f = 1 kHz$ $I_D = 250 mA$; $V_{DS} = 20 V$	$ y_{fs} $	typ.	400 mS
Input capacitance at $f = 1 MHz$ $V_{DS} = 10 V$; $V_{GS} = 0$	C_{is}	typ. <	75 pF 100 pF
Output capacitance at $f = 1 MHz$ $V_{DS} = 10 V$; $V_{GS} = 0$	C_{os}	typ. <	25 pF 35 pF
Feedback capacitance at $f = 1 MHz$ $V_{DS} = 10 V$; $V_{GS} = 0$	C_{rs}	typ. <	3 pF 5 pF
Switching times (see Figs 2 and 3) $I_D = 100 mA$; $V_{DS} = 200 V$; $V_{GS} = 0$ to 10 V	t_{on}	<	10 ns
	t_{off}	<	100 ns

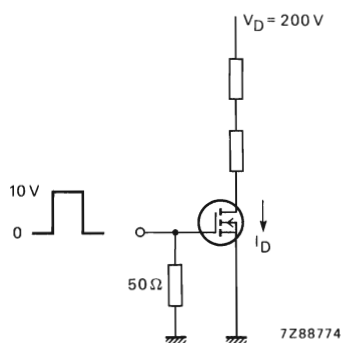


Fig. 2 Switching times test circuit.

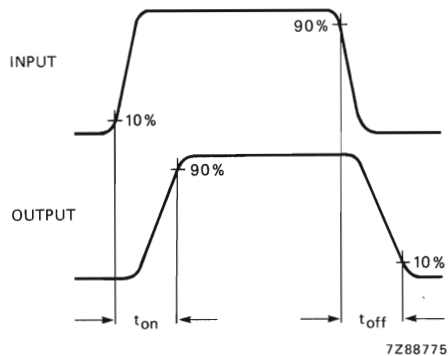


Fig. 3 Input and output waveforms.

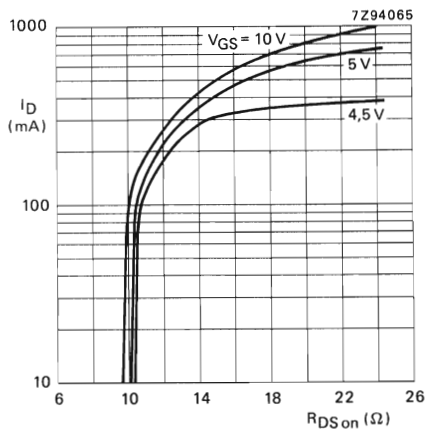
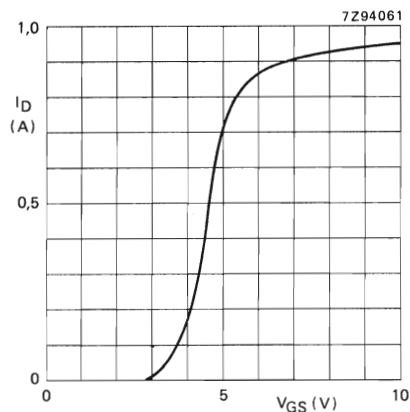
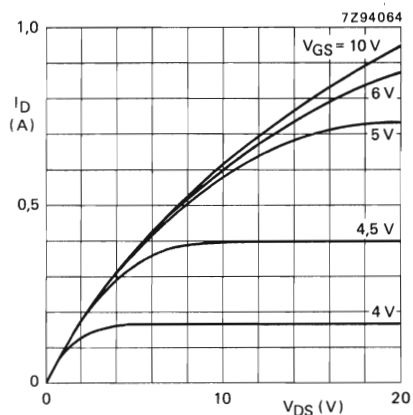
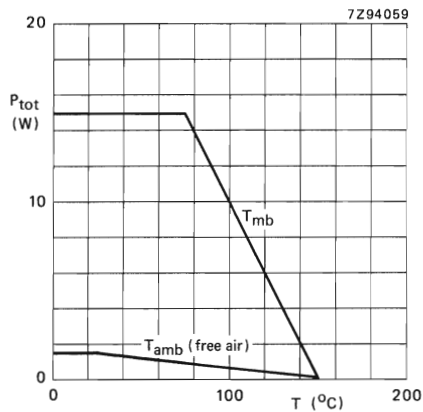
Fig. 4 $T_j = 25\text{ }^{\circ}\text{C}$; typical values.Fig. 5 $T_j = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 20\text{ V}$; typical values.Fig. 6 $T_j = 25\text{ }^{\circ}\text{C}$; typical values.

Fig. 7 Power derating curve.

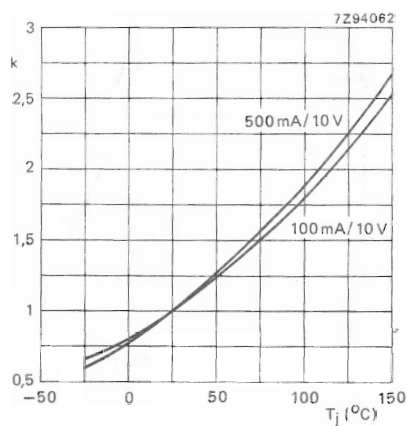


Fig. 8 $k = \frac{R_{DS\text{ on at } T_j}}{R_{DS\text{ on at } 25^\circ\text{C}}}$; typical values.

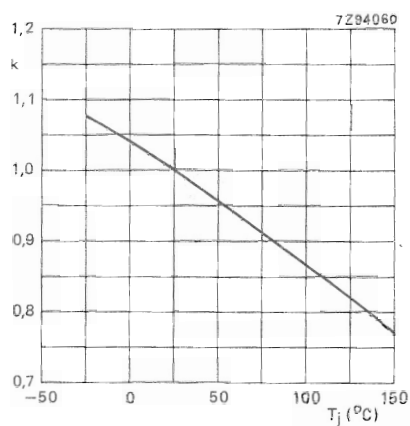


Fig. 9 $k = \frac{V_{GS(th) \text{ at } T_j}}{V_{GS(th) \text{ at } 25^\circ\text{C}}}$; $V_{GS(th)}$ at 1 mA; typical values.

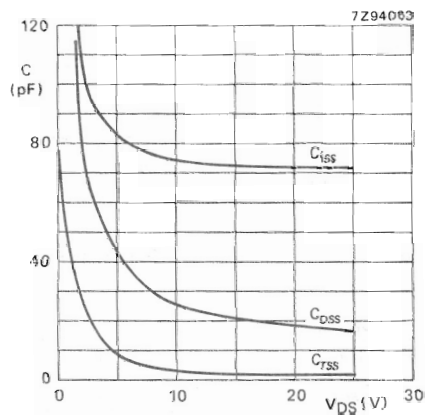


Fig. 10 $T_j = 25^\circ\text{C}$; $V_{GS} = 0$; $f = 1\text{ MHz}$; typical values.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT-89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

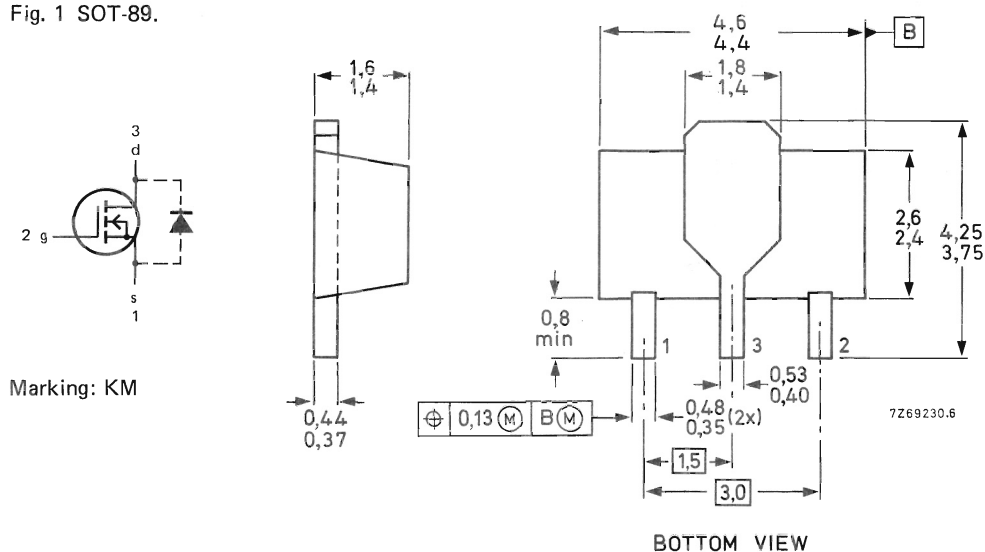
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,5 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	1 W
Drain-source ON-resistance $I_D = 500\text{ mA}$; $V_{GS} = 10\text{ V}$	R_{DSon}	typ. <	2,0 Ω 4,0 Ω
Transfer admittance $I_D = 500\text{ mA}$; $V_{DS} = 15\text{ V}$; $f = 1\text{ kHz}$	$ y_{fs} $	typ.	300 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-89.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,5 A
Drain current (peak)	I_{DM}	max.	1,0 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	1 W
Storage temperature	T_{stg}	–65 to + 150	$^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$	125 K/W
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CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Drain-source breakdown voltage

$I_D = 100\text{ }\mu\text{A}; V_{GS} = 0$	$V_{(BR)DS}$	>	80 V
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Drain-source leakage current

$V_{DS} = 60\text{ V}; V_{GS} = 0$	I_{DSS}	<	10 μA
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Gate-source leakage current

$V_{GS} = 20\text{ V}; V_{DS} = 0$	I_{GSS}	<	100 nA
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Gate threshold voltage

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$V_{GS(th)}$	>	1,5 V
		<	3,5 V

Drain-source ON-resistance

$I_D = 500\text{ mA}; V_{GS} = 10\text{ V}$	R_{DSon}	typ.	2,0 Ω
		<	4,0 Ω

Transfer admittance at $f = 1\text{ kHz}$

$I_D = 500\text{ mA}; V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	300 mS
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Input capacitance at $f = 1\text{ MHz}$

$V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{is}	typ.	45 pF
		<	60 pF

Output capacitance at $f = 1\text{ MHz}$

$V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{os}	typ.	30 pF
		<	45 pF

Feedback capacitance at $f = 1\text{ MHz}$

$V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{rs}	typ.	8 pF
		<	12 pF

Switching times (see Figs 2 and 3)

$I_D = 500\text{ mA}; V_{DS} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$	t_{on}	<	10 ns
	t_{off}	<	15 ns

* Transistors mounted on a substrate with surface area of 2,5 cm² and thickness of 0,7 mm.

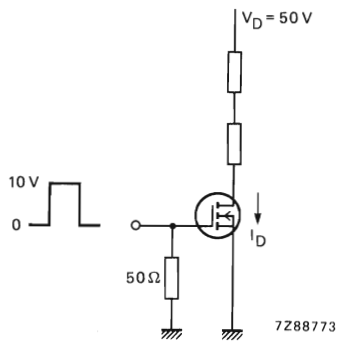


Fig. 2 Switching times test circuit.

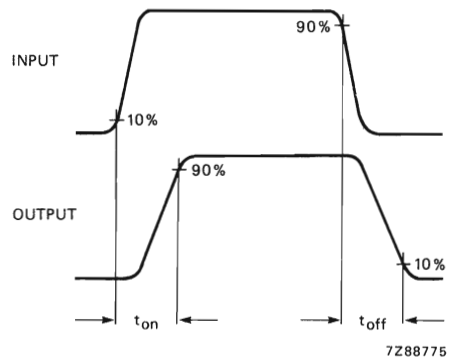


Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT-23 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for telephone ringer and for application with relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

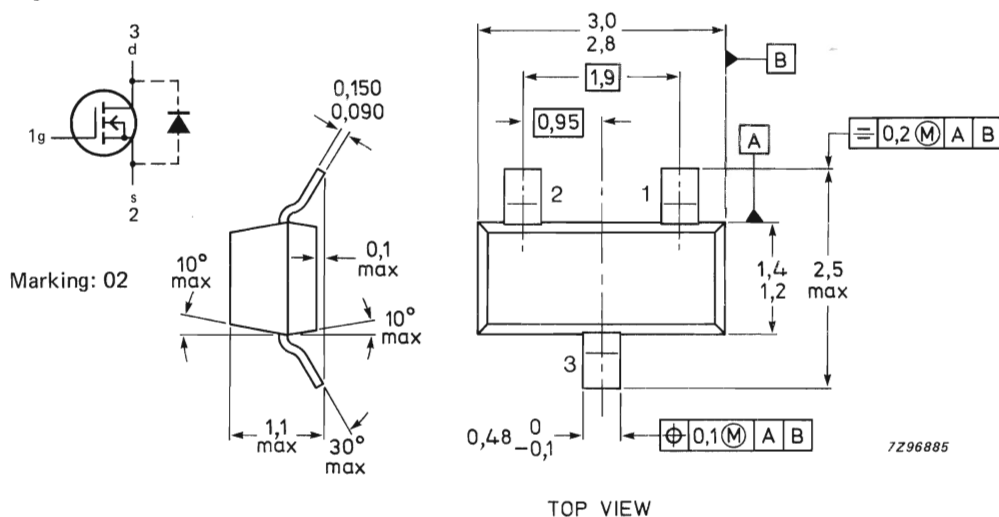
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	175 mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	300 mW
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	$R_{DS(on)}$	typ. <	7 Ω 10 Ω
Transfer admittance $I_D = 175$ mA; $V_{DS} = 5$ V; $f = 1$ kHz	$ y_{fs} $	typ.	150 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	V_{GS0}	max.	20 V
Drain current (d.c.)	I_D	max.	175 mA
Drain current (peak)	I_{DM}	max.	600 mA
Total power dissipation up to $T_{amb} = 25$ °C*	P_{tot}	max.	300 mW
Storage temperature range	T_{stg}	–65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$	=	430 K/W
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CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified

Drain-source breakdown voltage $I_D = 100$ μ A; $V_{GS} = 0$	$V_{(BR)DS}$	>	80 V
Drain-source leakage current $V_{DS} = 60$ V; $V_{GS} = 0$	I_{DSS}	<	1,0 μ A
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	<	100 nA
Gate-source cut-off voltage $I_D = 1$ mA; $V_{DS} = V_{GS}$	$V_{(P)GS}$	> <	1,5 V 3,5 V
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	R_{DSon}	typ. <	7 Ω 10 Ω
Transfer admittance at $f = 1$ kHz $I_D = 175$ mA; $V_{DS} = 5$ V	$ y_{fs} $	typ.	150 mS
→ Input capacitance at $f = 1$ MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ. <	15 pF 30 pF
→ Output capacitance at $f = 1$ MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ. <	13 pF 20 pF
→ Feedback capacitance at $f = 1$ MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ. <	3 pF 6 pF
Switching times (see Figs 2 and 3) $I_D = 175$ mA; $V_{DS} = 50$ V; $V_{GS} = 0$ to 10 V	t_{on}	typ. <	4 ns 10 ns
	t_{off}	typ. <	4 ns 10 ns

* Transistors mounted on a ceramic substrate of 7 mm x 5 mm x 0,7 mm.

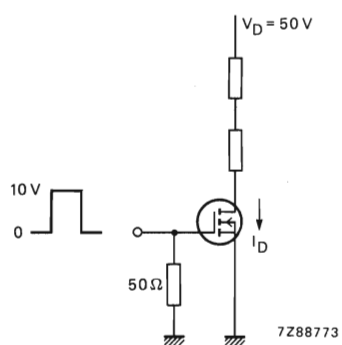


Fig. 2 Switching times test circuit.

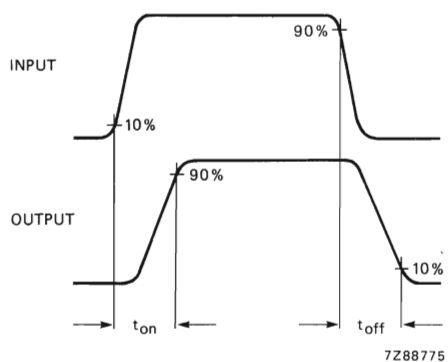


Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in SOT-89 envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	250 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	1 W
Drain-source ON-resistance $I_D = 250\text{ mA}$; $V_{GS} = 10\text{ V}$	R_{DSon}	typ. <	6 Ω 12 Ω
Transfer admittance $I_D = 250\text{ mA}$; $V_{DS} = 15\text{ V}$; $f = 1\text{ kHz}$	$ y_{fs} $	typ.	250 mS

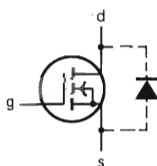
MECHANICAL DATA

Dimensions in mm

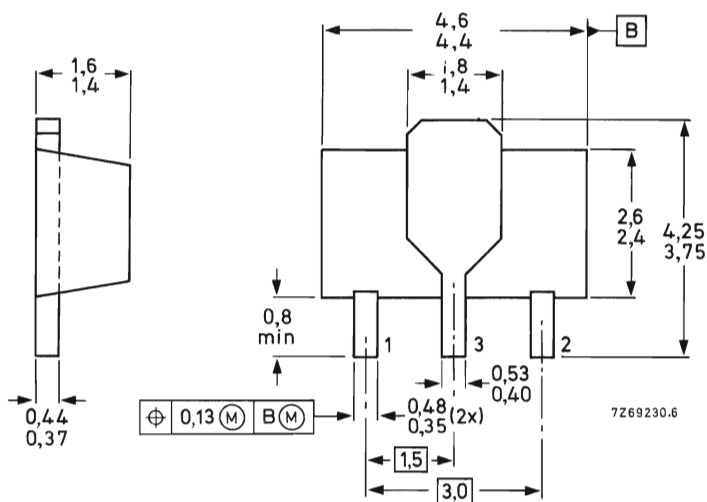
Fig. 1 SOT-89.

Pinning:

- 1 = source
2 = gate
3 = drain



Marking: KN



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	1 W
Storage temperature	T_{stg}	—65 to + 150	$^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	125 K/W
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CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Drain-source breakdown voltage

$$I_D = 100\text{ }\mu\text{A}; V_{GS} = 0$$

$$V_{(BR)DS} > 200\text{ V}$$

Drain-source leakage current

$$V_{DS} = 160\text{ V}; V_{GS} = 0$$

$$I_{DSS} < 10\text{ }\mu\text{A}$$

Gate-source leakage current

$$V_{GS} = 20\text{ V}; V_{DS} = 0$$

$$I_{GSS} < 100\text{ nA}$$

Gate threshold voltage

$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

$$V_{GS(th)} > 0,8\text{ V}$$

$$< 2,8\text{ V}$$

Drain-source ON-resistance

$$I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$$

$$R_{DSon} \text{ typ. } 6\text{ }\Omega$$

$$< 12\text{ }\Omega$$

Transfer admittance at $f = 1\text{ kHz}$

$$I_D = 250\text{ mA}; V_{DS} = 15\text{ V}$$

$$|y_{fs}| \text{ typ. } 250\text{ mS}$$

Input capacitance at $f = 1\text{ MHz}$

$$V_{DS} = 10\text{ V}; V_{GS} = 0$$

$$C_{is} \text{ typ. } 70\text{ pF}$$

$$< 90\text{ pF}$$

Output capacitance at $f = 1\text{ MHz}$

$$V_{DS} = 10\text{ V}; V_{GS} = 0$$

$$C_{os} \text{ typ. } 20\text{ pF}$$

$$< 30\text{ pF}$$

Feedback capacitance at $f = 1\text{ MHz}$

$$V_{DS} = 10\text{ V}; V_{GS} = 0$$

$$C_{rs} \text{ typ. } 5\text{ pF}$$

$$< 10\text{ pF}$$

Switching times (see Figs 2 and 3)

$$I_D = 250\text{ mA}; V_D = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$$

$$t_{on} \text{ typ. } 4\text{ ns}$$

$$< 10\text{ ns}$$

$$t_{off} \text{ typ. } 15\text{ ns}$$

$$< 25\text{ ns}$$

* Transistor mounted on a ceramic substrate with area of $2,5\text{ cm}^2$ and thickness of $0,7\text{ mm}$.

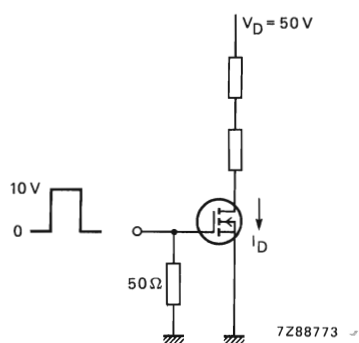


Fig. 2 Switching times test circuit.

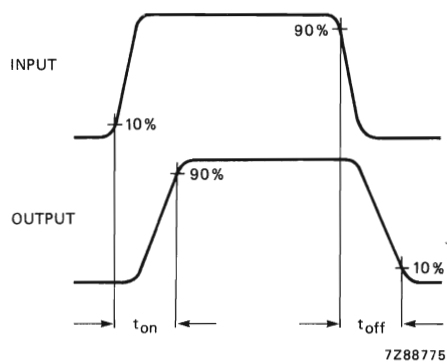


Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT-89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

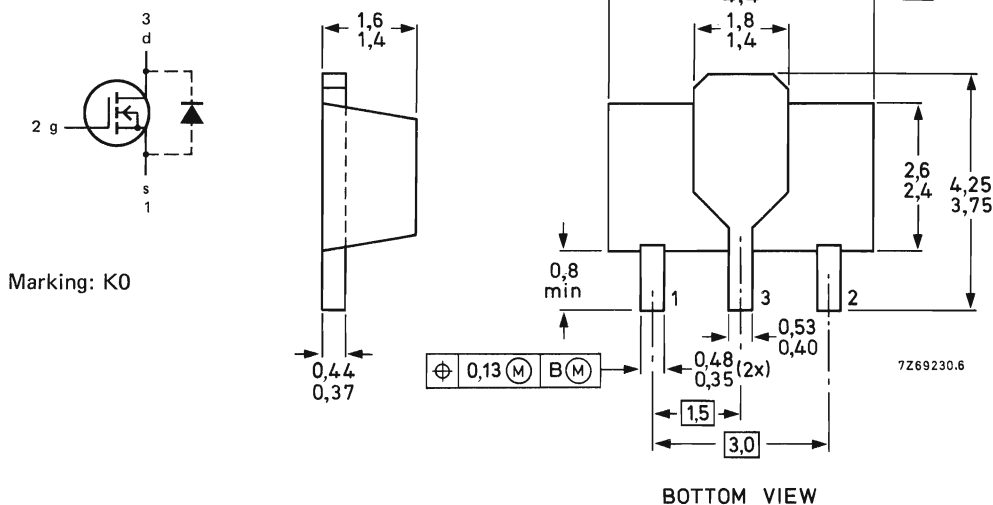
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	300 mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	1 W
Drain-source ON-resistance	R_{DSon}	typ.	7 Ω
$I_D = 15$ mA; $V_{GS} = 3$ V		<	10 Ω
Transfer admittance	$ y_{fs} $	typ.	250 mS
$I_D = 300$ mA; $V_{DS} = 15$ V; $f = 1$ kHz			

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-89.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to $T_{amb} = 25$ °C*	P_{tot}	max.	1 W
Storage temperature	T_{stg}	–65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$	=	125 K/W
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CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified

Drain-source breakdown voltage $I_D = 100$ μ A; $V_{GS} = 0$	$V_{(BR)DS}$	>	180 V
Drain-source leakage current $V_{DS} = 120$ V; $V_{GS} = 0$	I_{DSS}	<	10 μ A
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	<	100 nA
Gate threshold voltage $I_D = 100$ μ A; $V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	0,7 V 2,7 V
Drain-source ON-resistance $I_D = 15$ mA; $V_{GS} = 3$ V	R_{DSon}	typ. <	7 Ω 10 Ω
$I_D = 300$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	6 Ω
Transfer admittance at $f = 1$ kHz $I_D = 300$ mA; $V_{DS} = 15$ V	$ y_{fs} $	typ.	250 mS
Input capacitance at $f = 1$ MHz → $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ. <	50 pF 65 pF
Output capacitance at $f = 1$ MHz → $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ. <	20 pF 30 pF
Feedback capacitance at $f = 1$ MHz → $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ. <	6 pF 10 pF
Switching times (see Figs 2 and 3) $I_D = 300$ mA; $V_D = 50$ V; $V_{GS} = 0$ to 10 V	t_{on} t_{off}	< <	10 ns 15 ns

* Transistors mounted on a ceramic substrate with area of 2,5 cm² and thickness of 0,7 mm.

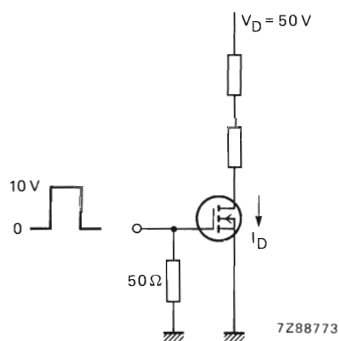


Fig. 2 Switching times test circuit.

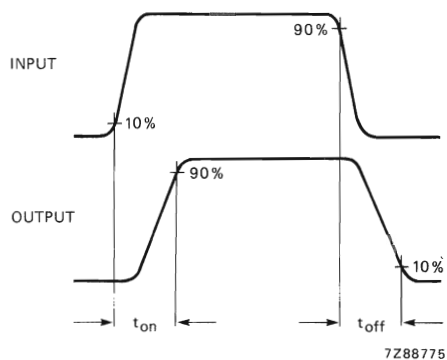


Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-39 envelope designed for application in motor controls, power supplies etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

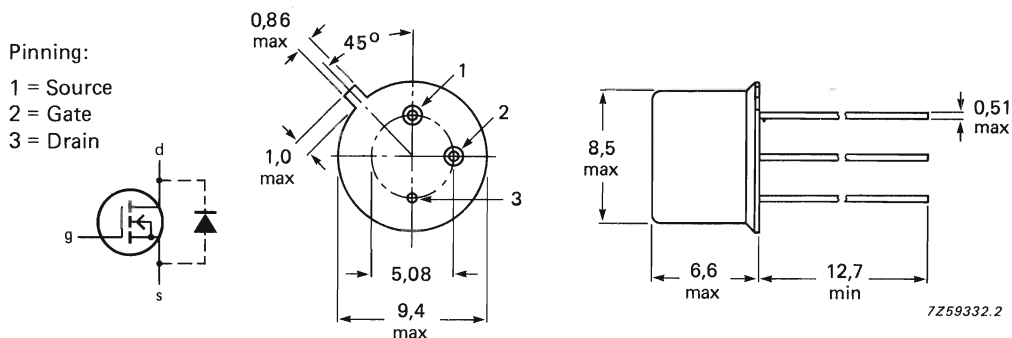
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	± 20 V
Drain current (d.c.)	I_D	max.	2,0 A
Total power dissipation up to $T_C = 25^\circ\text{C}$	P_{tot}	max.	10 W
Drain-source on-state resistance $I_D = 1,5$ A; $V_{GS} = 10$ V	$R_{DS(ON)}$	typ. <	1,8 Ω 2,0 Ω
Transfer admittance $I_D = 1,5$ A; $V_{DS} = 25$ V; $f = 1$ kHz	$ y_{fs} $	typ.	0,8 S

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-39.



Accessories: 56245 (distance disc)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	± 20 V
Drain current (d.c.)	I_D	max.	2,0 A
Drain current (peak)	I_{DM}	max.	5,0 A
Total power dissipation up to $T_C = 25^\circ\text{C}$	P_{tot}	max.	10 W
Storage temperature range	T_{stg}		-65 to $+150^\circ\text{C}$
Junction temperature	T_j	max.	150°C

THERMAL RESISTANCE

From junction to case	$R_{th\ j-c}$		12,5 K/W
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CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

Drain-source breakdown voltage

$I_D = 100\ \mu\text{A}; V_{GS} = 0$	$V_{(BR)DS}$	$>$	200 V
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Drain-source leakage current

$V_{DS} = 160\text{ V}; V_{GS} = 0$	I_{DSS}	$<$	10 μA
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Gate-source leakage current

$V_{GS} = 20\text{ V}; V_{DS} = 0$	I_{GSS}	$<$	100 nA
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Gate threshold voltage

$I_D = 1,0\text{ mA}; V_{DS} = V_{GS}$	$V_{GS(th)}$	$>$ $<$	1,0 V 3,0 V
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Drain-source on-state resistance

$I_D = 1,5\text{ A}; V_{GS} = 10\text{ V}$	$R_{DS(ON)}$	typ. $<$	1,8 Ω 2,0 Ω
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Transfer admittance at $f = 1\text{ kHz}$

$I_D = 1,5\text{ A}; V_{DS} = 25\text{ V}$	$ y_{fs} $	typ.	0,8 S
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Input capacitance at $f = 1\text{ MHz}$

$V_{DS} = 25\text{ V}; V_{GS} = 0$	C_{iss}	typ.	120 pF
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Output capacitance at $f = 1\text{ MHz}$

$V_{DS} = 25\text{ V}; V_{GS} = 0$	C_{oss}	typ.	40 pF
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Feedback capacitance at $f = 1\text{ MHz}$

$V_{DS} = 25\text{ V}; V_{GS} = 0$	C_{rss}	typ.	9 pF
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Switching times

$I_D = 1,5\text{ A}; V_D = 75\text{ V}; V_{GS} = 0$ to 10 V	t_{on}	$<$	35 ns
	t_{off}	$<$	50 ns

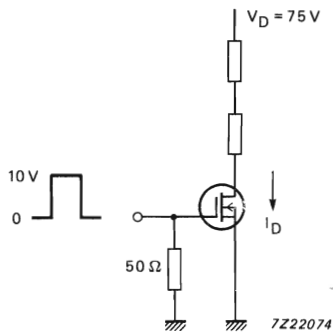


Fig. 2 Switching times test circuit.

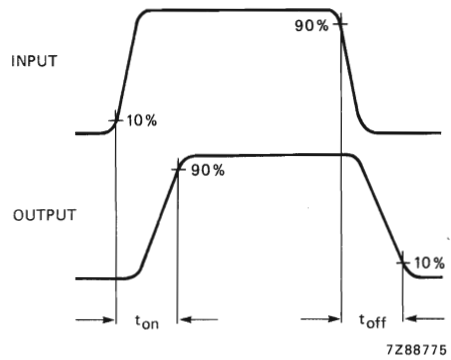


Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-18 and designed for use as line current interrupter in telephone sets and for application in relay, high speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

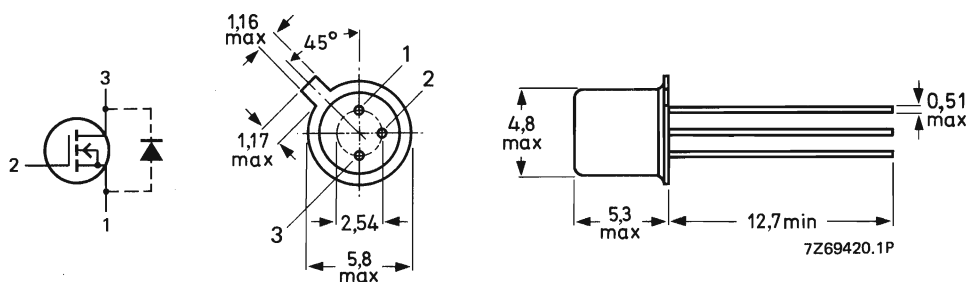
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p < 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	300 mA
Total power dissipation up to $T_C = 25^\circ C$	P_{tot}	max.	1,5 W
Drain-source ON-resistance $I_D = 300$ mA; $V_{GS} = 10$ V	$R_{DS(on)}$	typ.	6 Ω
Transfer admittance $I_D = 300$ mA; $V_{DS} = 15$ V; $f = 1$ kHz	$ y_{fs} $	typ.	250 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p < 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	0,4 W
Total power dissipation up to $T_C = 25$ °C	P_{tot}	max.	1,5 W
Storage temperature	T_{stg}	—65 to +150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	310 K/W
From junction to case	$R_{th\ j-c}$	83 K/W

CHARACTERISTICS $T_j = 25$ °C unless otherwise specified

Drain-source breakdown voltage

$I_D = 100\ \mu A; V_{GS} = 0$

$V_{(BR)DS} > 180\ V$

Drain-source leakage current

$V_{DS} = 120\ V; V_{GS} = 0$

$I_{DSS} < 10\ \mu A$

Gate-source leakage current

$V_{GS} = 20\ V; V_{DS} = 0$

$I_{GSS} < 100\ nA$

Gate threshold voltage

$I_D = 100\ \mu A; V_{DS} = V_{GS}$

$$V_{GS(th)} > 0,7\ V$$

$$< 2,7\ V$$

Drain-source ON-resistance (see Fig. 4)

$I_D = 15\ mA; V_{GS} = 3\ V$

$$R_{DSon} \text{ typ. } 7\ \Omega$$

$$< 10\ \Omega$$

$I_D = 300\ mA; V_{GS} = 10\ V$

$R_{DSon} \text{ typ. } 6\ \Omega$

Transfer admittance at $f = 1$ kHz

$I_D = 300\ mA; V_{DS} = 15\ V$

$|y_{fs}| \text{ typ. } 250\ mS$

Input capacitance at $f = 1$ MHz

$V_{DS} = 10\ V; V_{GS} = 0$

$$C_{is} \text{ typ. } 50\ pF$$

$$< 60\ pF$$

Output capacitance at $f = 1$ MHz

$V_{DS} = 10\ V; V_{GS} = 0$

$$C_{os} \text{ typ. } 20\ pF$$

$$< 30\ pF$$

Feedback capacitance at $f = 1$ MHz

$V_{DS} = 10\ V; V_{GS} = 0$

$$C_{rs} \text{ typ. } 6\ pF$$

$$< 10\ pF$$

Switching times (see Figs 2 and 3)

$I_D = 300\ mA; V_D = 50\ V; V_{GS} = 0 \text{ to } 10\ V$

$$t_{on} < 10\ ns$$

$$t_{off} < 15\ ns$$

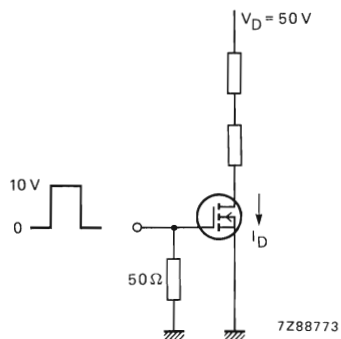


Fig. 2 Switching times test circuit.

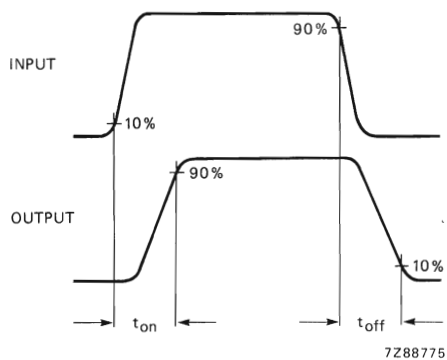
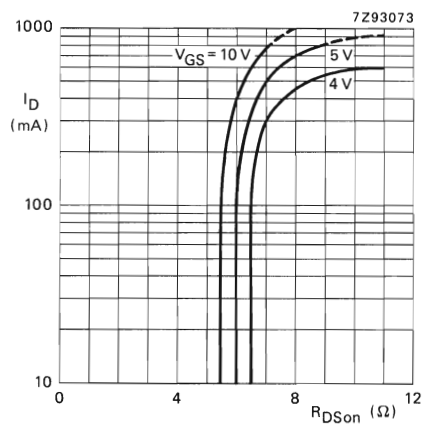


Fig. 3 Input and output waveforms.

Fig. 4 $T_j = 25^\circ C$; typ. values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features:

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

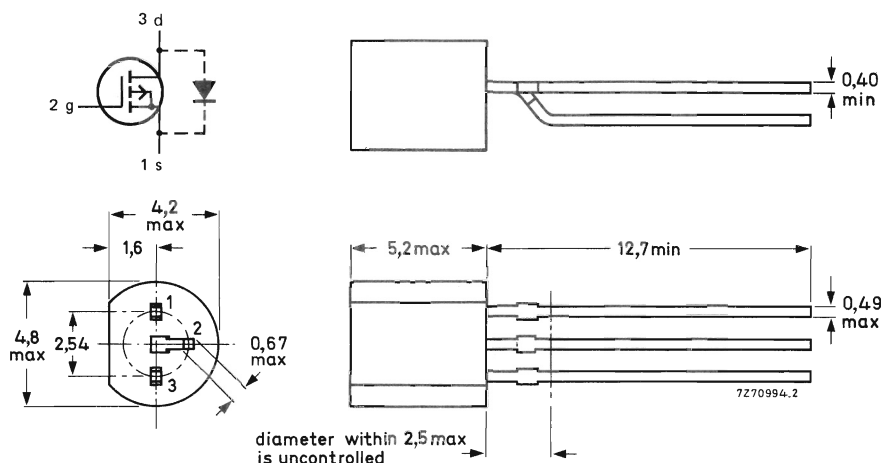
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,3 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	R_{DSon}	typ. max.	4,5 Ω 6 Ω
Transfer admittance $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	typ.	200 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,3 A
Drain current (peak)	$-I_{DM}$	max.	0,8 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	1 W
Storage temperature	T_{stg}		$-65\text{ to }+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$	125 K/W
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CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Drain-source breakdown voltage $-I_D = 100\text{ }\mu\text{A}; -V_{GS} = 0$	$-V_{(BR)DS}$	$>$	60 V
Drain-source leakage current $-V_{DS} = 45\text{ V}; V_{GS} = 0$	$-I_{DSS}$	$<$	10 μA
Gate-source leakage current $-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	$<$	100 nA
Gate threshold voltage $-I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$-V_{GS(th)}$	$>$ $<$	1,5 V 3,5 V
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	R_{DSon}	typ. $<$	4,5 Ω 6 Ω
Transfer admittance at $f = 1\text{ kHz}$ $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	200 mS
Input capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{is}	typ. $<$	55 pF 70 pF
→ Output capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{os}	typ. $<$	30 pF 45 pF
→ Feedback capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{rs}	typ. $<$	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D = 200\text{ mA}; -V_D = 50\text{ V}; -V_{GS} = 0\text{ to }10\text{ V}$	t_{on} t_{off}	typ. typ.	4 ns 20 ns

* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

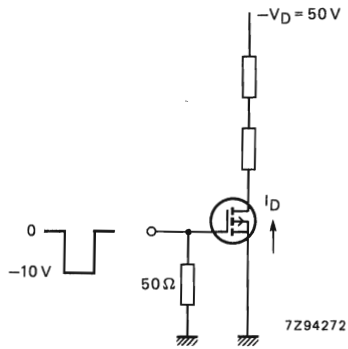


Fig. 2 Switching times test circuit.

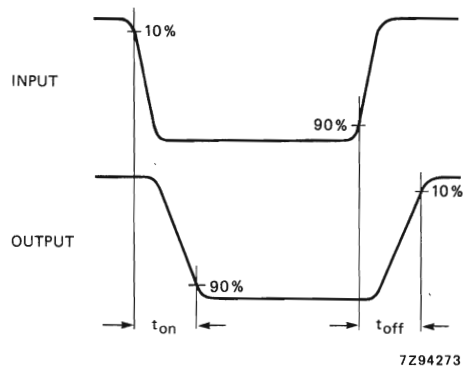


Fig. 3 Input and output waveforms.

P-CHANNEL VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

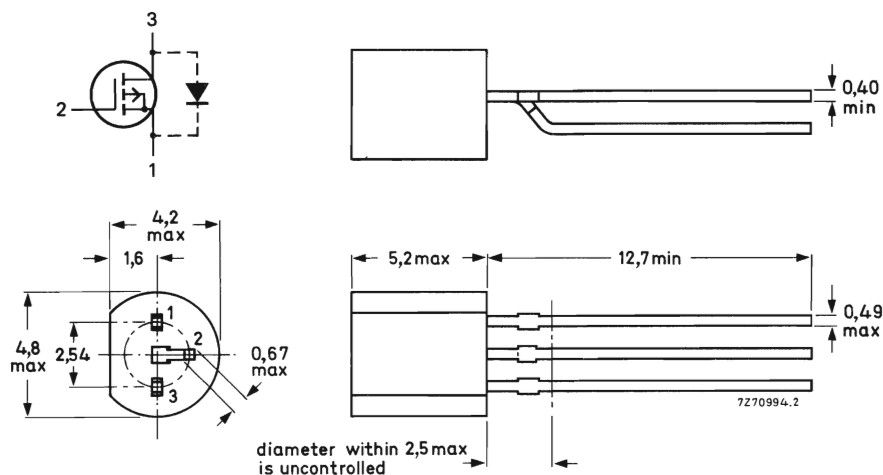
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	50 V
Gate-source voltage (open drain)	$-V_{GS0}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,25 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	0,83 W
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	R_{DSon}	typ. <	7,5 Ω 10 Ω
Transfer admittance at $f = 1\text{ kHz}$ $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	125 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	50 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,25 A
Drain current (peak)	$-I_{DM}$	max.	0,5 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	0,83 W
Storage temperature	T_{stg}		$-65\text{ to }+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$	=	150 K/W
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CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Drain-source breakdown voltage $-I_D = 100\text{ }\mu\text{A}; V_{GS} = 0$	$-V_{(BR)DS}$	>	50 V
Drain-source leakage current $-V_{DS} = 40\text{ V}; V_{GS} = 0$	$-I_{DSS}$	<	10 μA
Gate-source leakage current $-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	100 nA
Gate threshold voltage $-I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$-V_{GS(th)}$	> <	1,5 V 3,5 V
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	R_{DSon}	typ. <	7,5 Ω 10 Ω
Transfer admittance at $f = 1\text{ kHz}$ $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	125 mS
Input capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{is}	typ.	30 pF
Output capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{os}	typ.	20 pF
Feedback capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{rs}	typ.	5 pF
Switching times (see Figs 2 and 3) $-I_D = 200\text{ mA}; -V_{DS} = 40\text{ V}; -V_{GS} = 0\text{ to }10\text{ V}$	t_{on} t_{off}	typ. typ.	4 ns 10 ns

* Transistor mounted on printed circuit board, max. lead length 4 mm.

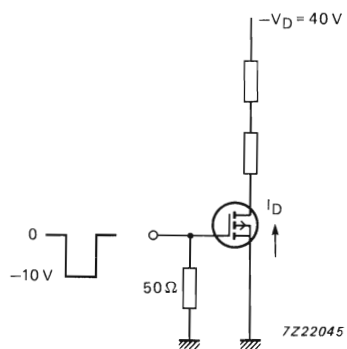


Fig. 2 Switching times test circuit.

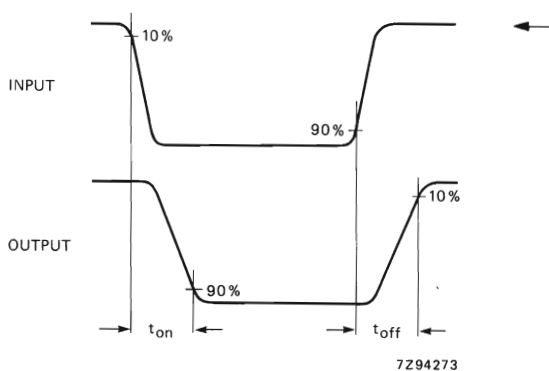


Fig. 3 Input and output waveforms.

P-CHANNEL VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT-89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD technology.

Features

- Very low $R_{DS(on)}$
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$-V_{GS}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,3 A
Total power dissipation up to $T_{amb} = 25^\circ\text{C}$	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ. max.	4,5 Ω 6 Ω
Transfer admittance $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	typ.	200 mS

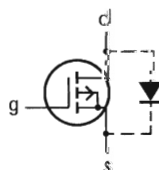
MECHANICAL DATA

Dimensions in mm

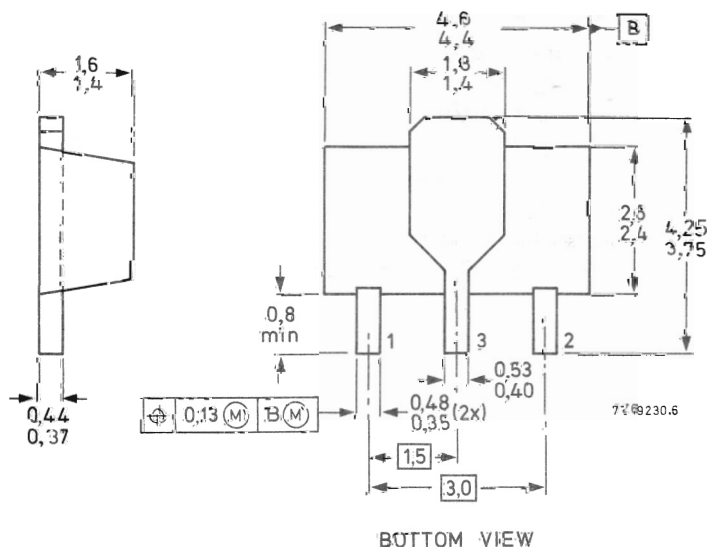
Fig. 1 SOT-89.

Pinning:

- 1 = source
2 = gate
3 = drain



marking: L:M



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$-V_{GS0}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,3 A
Drain current (peak)	$-I_{DM}$	max.	0,8 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}^*$	P_{tot}	max.	1 W
Storage temperature	T_{stg}		$-65\text{ to }+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	150 $^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$	=	125 K/W
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CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Drain-source breakdown voltage $-I_D = 100\text{ }\mu\text{A}; -V_{GS} = 0$	$-V_{(BR)DS}$	>	60 V
Drain-source leakage current $-V_{DS} = 45\text{ V}; V_{GS} = 0$	$-I_{DSS}$	<	10 μA
Gate-source leakage current $-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	100 nA
Gate threshold voltage $-I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$-V_{GS(th)}$	> <	1,5 V 3,5 V
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	R_{DSon}	typ. <	4,5 Ω 6 Ω
Transfer admittance at $f = 1\text{ kHz}$ $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	200 mS
Input capacitance at $f = 1\text{ MHz}$ → $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{is}	typ. <	55 pF 70 pF
Output capacitance at $f = 1\text{ MHz}$ → $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{os}	typ. <	30 pF 45 pF
Feedback capacitance at $f = 1\text{ MHz}$ → $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{rs}	typ. <	8 pF 12 pF
Switching times (see Figs 2 and 3) → $-I_D = 200\text{ mA}; -V_D = 50\text{ V}; -V_{GS} = 0\text{ to }10\text{ V}$	t_{on} t_{off}	typ. typ.	4 ns 20 ns

* Transistor mounted on a ceramic substrate: area = 2,5 cm² and thickness = 0,7 mm.

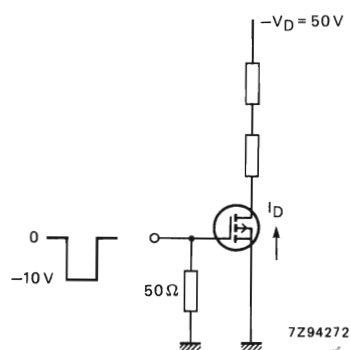


Fig. 2 Switching time test circuit.

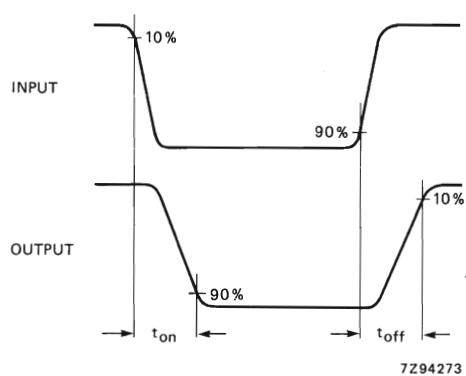


Fig. 3 Input and output waveforms.

P-CHANNEL VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT-89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD-technology.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL
- High-speed switching
- No second breakdown

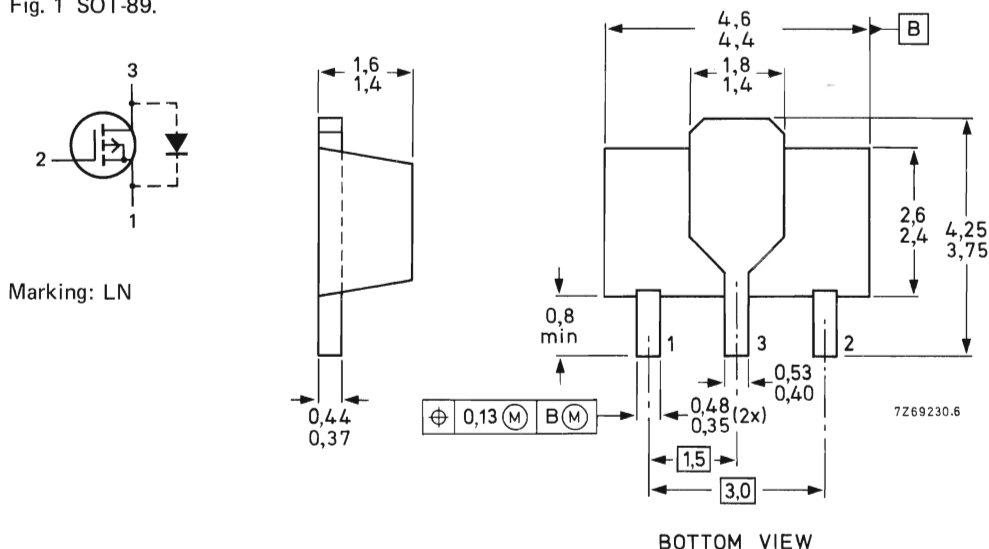
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	50 V
Gate-source voltage (open drain)	$-V_{GS}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,25 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	R_{DSon}	typ. max.	7,5 Ω 10 Ω
Transfer admittance $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}; f = 1\text{ kHz}$	$ y_{fs} $	typ.	125 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-89.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	50 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20 V
Drain current (d.c.)	$-I_D$	max.	0,25 A
Drain current (peak)	$-I_{DM}$	max.	0,5 A
Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	1 W
Storage temperature	T_{stg}		-65 to $+150\text{ }^{\circ}\text{C}$
Junction temperature	T_j	max.	$150\text{ }^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$	=	125 K/W
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CHARACTERISTICS $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Drain-source breakdown voltage $-I_D = 100\text{ }\mu\text{A}; -V_{GS} = 0$	$-V_{(BR)DS}$	>	50 V
Drain-source leakage current $-V_{DS} = 1\text{ V}; V_{GS} = 0$	$-I_{DSS}$	<	10 μA
Gate-source leakage current $-V_{GS} = 20\text{ V}; V_{DS} = 0$	$-I_{GSS}$	<	100 nA
Gate threshold voltage $-I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$-V_{GS(th)}$	> <	1,5 V 3,5 V
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	R_{DSon}	typ. <	7,5 Ω 10 Ω
Transfer admittance at $f = 1\text{ kHz}$ $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	125 mS
→ Input capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{is}	typ. <	30 pF 45 pF
→ Output capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{os}	typ. <	20 pF 30 pF
→ Feedback capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{rs}	typ. <	5 pF 10 pF
→ Switching times (see Figs 2 and 3) $-I_D = 200\text{ mA}; -V_D = 50\text{ V}; -V_{GS} = 0$ to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

* Transistor mounted on a ceramic substrate: area = $2,5\text{ cm}^2$; thickness = $0,7\text{ mm}$.

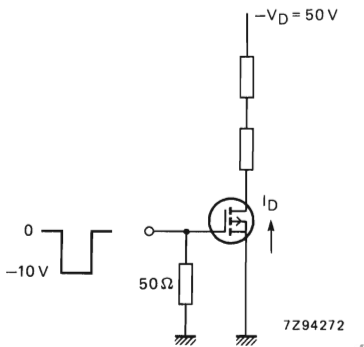


Fig. 2 Switching times test circuit.

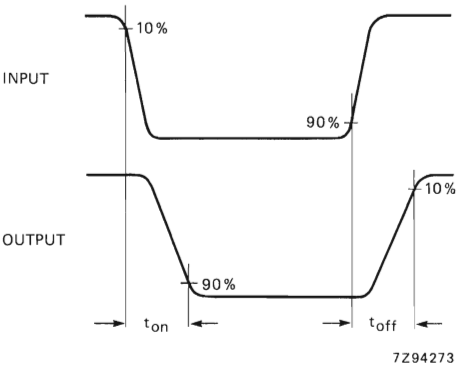


Fig. 3 Input and output waveforms.

DEVELOPMENT DATA

N-CHANNEL VERTICAL D-MOS TRANSISTORS

N-channel enhancement mode vertical D-MOS transistors, in TO-92 variant envelopes and designed for application as low power, high-frequency inverters and line drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS(on)}$

QUICK REFERENCE DATA

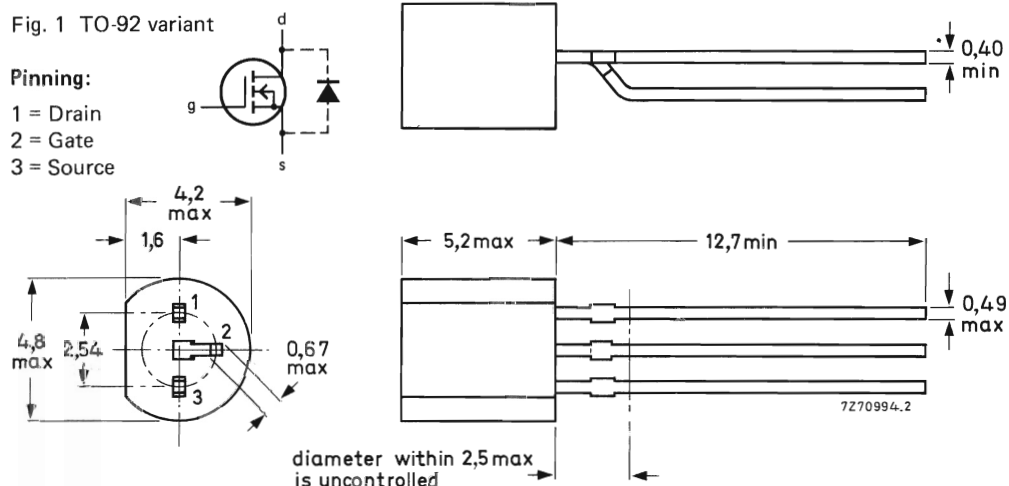
			PH6659	PH6660	PH6661
Drain-source voltage	V_{DS}	max.	35	60	90 V
Gate-source voltage (open drain)	V_{GSO}	max.	20	20	20 V
Drain current (d.c.)	I_D	max.	0,75	0,5	0,5 A
Total power dissipation up to $T_{amb} = 25^\circ\text{C}$	P_{tot}	max.	1	1	1 W
Drain-source on-state resistance $I_D = 1,0\text{ A}; V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ. <	0,9 1,8	1,4 3,0	1,9 Ω 4,0 Ω
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 0,5\text{ A}; V_{DS} = 25\text{ V}$	$ y_{fs} $	>	170	170	170 mS

MECHANICAL DATA

Fig. 1 TO-92 variant

Pinning:

- 1 = Drain
2 = Gate
3 = Source



Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			PH6659	PH6660	PH6661
Drain-source voltage	V_{DS}	max.	35	60	90 V
Gate-source voltage (open drain)	V_{GSO}	max.	20	20	20 V
Drain current (d.c.)	I_D	max.	0,75	0,5	0,5 A
Drain current (peak)	I_{DM}	max.		1,0	A
Total power dissipation up to $T_{amb} = 25\text{ °C}$	P_{tot}	max.		1	W
Storage temperature	T_{stg}			-65 to +150	°C
Junction temperature	T_j	max.		150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j-a}$		125	K/W
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CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified

			PH6659	PH6660	PH6661
Drain-source breakdown voltage $I_D = 10\text{ }\mu\text{A}$; $V_{GS} = 0$	$V_{(BR)DSS}$	>	35	60	90 V
Drain-source leakage current at $V_{DS} = V_{DS\text{ max}}$; $V_{GS} = 0$	I_{DSS}	<	10	10	10 μA
Gate-source leakage current at $V_{GS} = 15\text{ V}$; $V_{DS} = 0$	I_{GSS}	<	100	100	100 nA
Gate threshold voltage $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	0,8 2,0	0,8 2,0	0,8 V 2,0 V
On-state drain current $V_{DS} = 25\text{ V}$; $V_{GS} = 10\text{ V}$	$I_{D(ON)}$	> typ.	1,0 2,0	1,0 2,0	1,0 A 2,0 A
Drain-source on-state resistance $I_D = 0,3\text{ A}$; $V_{GS} = 5\text{ V}$	$R_{DS(on)}$	typ. <	1,5 5,0	1,8 5,0	2,4 Ω 5,3 Ω
$I_D = 1,0\text{ A}$; $V_{GS} = 10\text{ V}$	$R_{DS(ON)}$	typ. <	0,9 1,8	1,4 3,0	1,9 Ω 4,0 Ω
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 0,5\text{ A}$; $V_{DS} = 25\text{ V}$	$ y_{fs} $	>	170	170	170 mS
Input capacitance at $f = 1\text{ MHz}$ $V_{DS} = 25\text{ V}$; $V_{GS} = 0$	C_{iss}	<	50	50	50 pF
Output capacitance at $f = 1\text{ MHz}$ $V_{DS} = 25\text{ V}$; $V_{GS} = 0$	C_{oss}	<	50	40	40 pF

* Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

Feedback capacitance at $f = 1 \text{ MHz}$

$$V_{DS} = 25 \text{ V}; V_{GS} = 0$$

 C_{rss}

<

15

15

15 pF

Switching times

$$I_D = 1.0 \text{ A}; V_D = 25 \text{ V};$$

$$V_{GS} = 0 \text{ to } 10 \text{ V}$$

 t_{on}

typ

5

5

5 ns

<

10

10

10 ns

 t_{off}

typ

5

5

5 ns

<

10

10

10 ns

DEVELOPMENT DATA

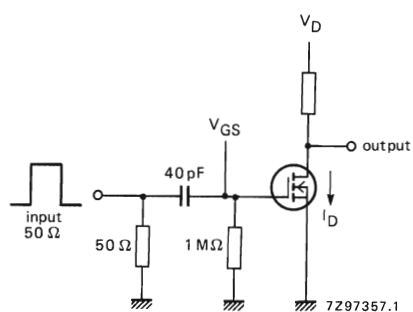


Fig. 2 Switching times test circuit.

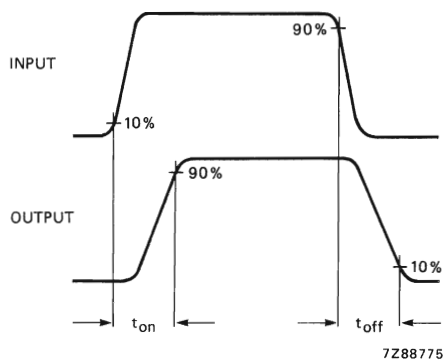


Fig. 3 Input and output waveforms.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-39 envelope and designed for application as low-power, high-frequency inverters and line drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low R_{DSon}

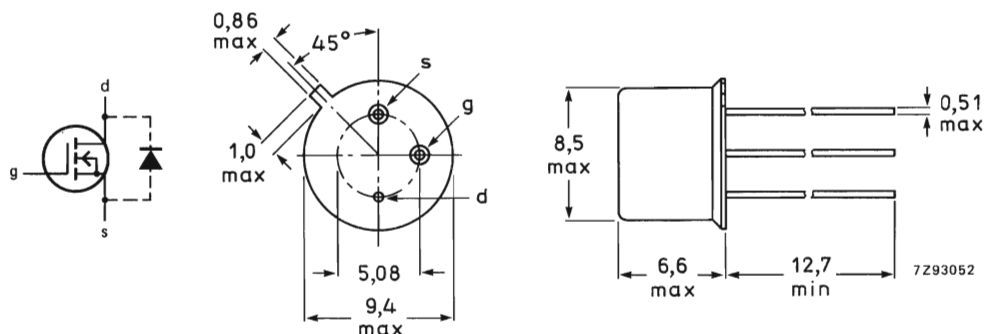
QUICK REFERENCE DATA

		2N6659	2N6660	2N6661
Drain-source voltage	V_{DS}	max. 35	60	90 V
Gate-source voltage (open drain)	V_{GSO}	max. 30	30	30 V
Drain current (d.c.)	I_D	max. 1,4	1,1	0,9 A
Total power dissipation up to $T_c = 25^\circ\text{C}$	P_{tot}	max. 6,25	6,25	6,25 W
Drain-source ON-resistance $I_D = 1,0\text{ A}; V_{GS} = 10\text{ V}$	R_{DSon}	typ. 0,9 < 1,8	1,4 3,0	1,9 Ω 4,0 Ω
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 0,5\text{ A}; V_{DS} = 25\text{ V}$	$ y_{fs} $	> 170	170	170 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-39.



Maximum lead diameter is guaranteed only for 12,7 mm

Accessories: 56245 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			2N6659	2N6660	2N6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
→ Gate-source voltage (open drain)	V_{GSO}	max.	30	30	30	V
Drain current (d.c.)	I_D	max.	1,4	1,1	0,9	A
Drain current (peak)*	I_{DM}	max.		3,0		A
Total power dissipation up to $T_C = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.		6,25		W
Storage temperature	T_{stg}			-65 to + 150		$^{\circ}\text{C}$
Junction temperature	T_j	max.		150		$^{\circ}\text{C}$
THERMAL RESISTANCE						
From junction to case	$R_{th\ j-c}$			20		K/W

CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

			2N6659	2N6660	2N6661	
Drain-source breakdown voltage $I_D = 10\text{ }\mu\text{A}; V_{GS} = 0$	$V_{(BR)DSS}$	>	35	60	90	V
Drain-source leakage current at $V_{DS} = V_{DSmax}; V_{GS} = 0$	I_{DSS}	<	10	10	10	μA
Gate-source leakage current at $V_{GS} = 15\text{ V}; V_{DS} = 0$	I_{GSS}	<	100	100	100	nA
Gate threshold voltage $I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$V_{GS(th)}$	> <	0,8 2,0	0,8 2,0	0,8 2,0	V V
ON-state drain current $V_{DS} = 25\text{ V}; V_{GS} = 10\text{ V}$	$I_{D(on)}$	> typ.	1,0 2,0	1,0 2,0	1,0 2,0	A A
Drain-source ON-resistance $I_D = 0,3\text{ A}; V_{GS} = 5\text{ V}$	R_{DSon}	typ. <	1,5 5,0	1,8 5,0	2,4 5,3	Ω Ω
$I_D = 1,0\text{ A}; V_{GS} = 10\text{ V}$	R_{DSon}	typ. <	0,9 1,8	1,4 3,0	1,9 4,0	Ω Ω
Transfer admittance at $f = 1\text{ kHz}$ $I_D = 0,5\text{ A}; V_{DS} = 25\text{ V}$	$ y_{fs} $	>	170	170	170	mS
Input capacitance at $f = 1\text{ MHz}$ $V_{DS} = 25\text{ V}; V_{GS} = 0$	C_{iss}	<	50	50	50	pF
Output capacitance at $f = 1\text{ MHz}$ $V_{DS} = 25\text{ V}; V_{GS} = 0$	C_{oss}	<	50	40	40	pF

* Pulse conditions: $t_p \leq 300\text{ }\mu\text{s}; \delta = 0,01$.

Feedback capacitance at $f = 1 \text{ MHz}$

$$V_{DS} = 25 \text{ V}; V_{GS} = 0$$

Switching times

$$I_D = 1.0 \text{ A}; V_D = 25 \text{ V};$$

$$V_{GS} = 0 \text{ to } 10 \text{ V}$$

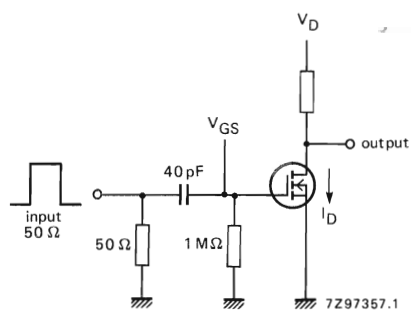


Fig. 2 Switching times test circuit.

		2N6659	2N6660	2N6661	
C_{rss}	<	15	15	15	pF
t_{on}	typ.	5	5	5	ns
	<	10	10	10	ns
t_{off}	typ.	5	5	5	ns
	<	10	10	10	ns

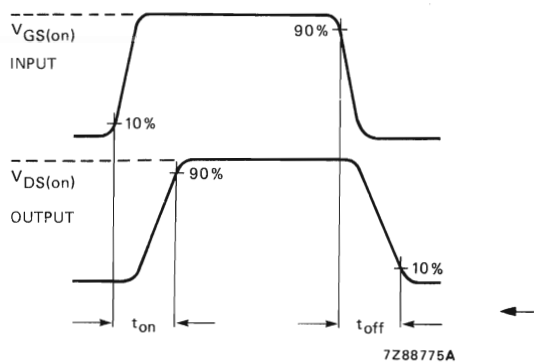
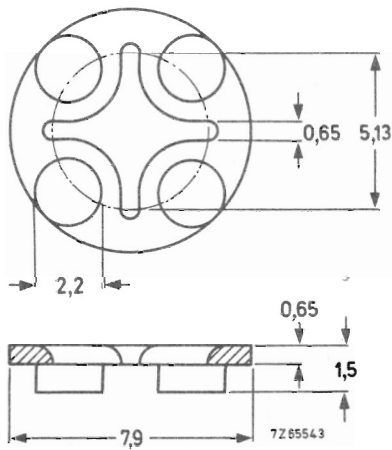


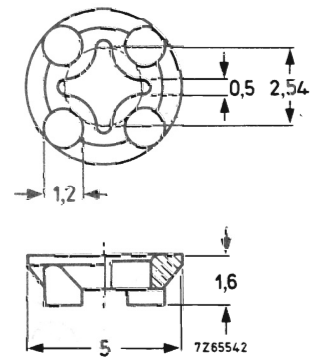
Fig. 3 Input and output waveforms.

MECHANICAL DATA

Dimensions in mm



Distance disc 56245 for TO-5 or TO-39;
insulating material.

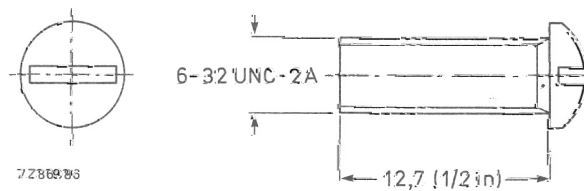


Distance disc 56246 for TO-18 or TO-72;
insulating material.

Maximum permissible temperature: 100 °C.

ROUND HEAD SCREW 6-32 UNC-2A

Available, upon request, under type number 56396 or 12 NC code number 9390 298 10xx.0.



INDEX OF TYPE NUMBERS

The inclusion of a type number in this publication does not necessarily imply its availability.

type no.	book	section	type no.	book	section	type no.	book	section
BA220	S1	SD	BAS29	S7/S1	Mm/SD	BAV99	S7/S1	Mm/SD
BA221	S1	SD	BAS31	S7/S1	Mm/SD	BAV100	S7/S1	Mm/SD
BA223	S1	T	BAS32	S7/S1	Mm/SD	BAV101	S7/S1	Mm/SD
BA281	S1	SD	BAS35	S7/S1	Mm/SD	BAV102	S7/S1	Mm/SD
BA314	S1	Vrg	BAS45	S1	SD	BAV103	S7/S1	Mm/SD
BA315	S1	Vrg	BAS56	S1/S7	SD/Mm	BAW56	S7/S1	Mm/SD
BA316	S1	SD	BAT17	S7/S1	Mm/T	BAW62	S1	SD
BA317	S1	SD	BAT18	S7/S1	Mm/T	BAX12	S1	SD
BA318	S1	SD	BAT54	S1/S7	SD/Mm	BAX14	S1	SD
BA423	S1	T	BAT74	S1/S7	SD/Mm	BAX18	S1	SD
BA480	S1	T	BAT81	S1	T	BAY80	S1	SD
BA481	S1	T	BAT82	S1	T	BB112	S1	T
BA482	S1	T	BAT83	S1	T	BB119	S1	T
BA483	S1	T	BAT85	S1	T	BB130	S1	T
BA484	S1	T	BAT86	S1	T	BB204B	S1	T
BA682	S1/S7	T/Mm	BAV10	S1	SD	BB204G	S1	T
BA683	S1/S7	T/Mm	BAV18	S1	SD	BB212	S1	T
BAS11	S1	SD	BAV19	S1	SD	BB215	S7/S1	Mm/SD
BAS15	S1	SD	BAV20	S1	SD	BB219	S7/S1	Mm/SD
BAS16	S7/S1	Mm/SD	BAV21	S1	SD	BB405B	S1	T
BAS17	S7/S1	Mm/Vrg	BAV23	S7/S1	Mm/SD	BB417	S1	T
BAS19	S7/S1	Mm/SD	BAV45	S1	Sp	BB809	S1	T
BAS20	S7/S1	Mm/SD	BAV45A	S1	Sp	BB909A	S1	T
BAS21	S7/S1	Mm/SD	BAV70	S7/S1	Mm/SD	BB909B	S1	T
BAS28	S7/S1	Mm/SD	BAV74	S1	SD	BBY31	S7/S1	Mm/T

Mm = Microminiature semiconductors
for hybrid circuits
SD = Small-signal diodes

Sp = Special diodes
T = Tuner diodes
Vrg = Voltage regulator diodes

type no.	book	section	type no.	book	section	type no.	book	section
BBY39	S1	T	BC639	S3	Sm	BCW69;R	S7	Mm
BBY40	S7/S1	Mm/T	BC640	S3	Sm	BCW70;R	S7	Mm
BC107	S3	Sm	BC807	S7	Mm	BCW71;R	S7	Mm
BC108	S3	Sm	BC808	S7	Mm	BCW72;R	S7	Mm
BC109	S3	Sm	BC817	S7	Mm	BCW81;R	S7	Mm
BC140	S3	Sm	BC818	S7	Mm	BCW89;R	S7	Mm
BC141	S3	Sm	BC846	S7	Mm	BCX17;R	S7	Mm
BC160	S3	Sm	BC847	S7	Mm	BCX18;R	S7	Mm
BC161	S3	Sm	BC848	S7	Mm	BCX19;R	S7	Mm
BC177	S3	Sm	BC849	S7	Mm	BCX20;R	S7	Mm
BC178	S3	Sm	BC850	S7	Mm	BCX51	S7	Mm
BC179	S3	Sm	BC856	S7	Mm	BCX52	S7	Mm
BC264A	S5	FET	BC857	S7	Mm	BCX53	S7	Mm
BC264B	S5	FET	BC858	S7	Mm	BCX54	S7	Mm
BC264C	S5	FET	BC859	S7	Mm	BCX55	S7	Mm
BC264D	S5	FET	BC860	S7	Mm	BCX56	S7	Mm
BC327;A	S3	Sm	BC868	S7	Mm	BCX58	S3	Sm
BC328	S3	Sm	BC869	S7	Mm	BCX59	S3	Sm
BC337;A	S3	Sm	BCF29;R	S7	Mm	BCX70*	S7	Mm
BC338	S3	Sm	BCF30;R	S7	Mm	BCX71*	S7	Mm
BC368	S3	Sm	BCF32;R	S7	Mm	BCX78	S3	Sm
BC369	S3	Sm	BCF33;R	S7	Mm	BCX79	S3	Sm
BC375	S3	Sm	BCF70;R	S7	Mm	BCY56	S3	Sm
BC376	S3	Sm	BCF81;R	S7	Mm	BCY57	S3	Sm
BC516	S3	Sm	BCV26	S7	Mm	BCY58	S3	Sm
BC517	S3	Sm	BCV27	S7	Mm	BCY59	S3	Sm
BC546	S3	Sm	BCV61	S7	Mm	BCY65	S3	Sm
BC547	S3	Sm	BCV62	S7	Mm	BCY70	S3	Sm
BC548	S3	Sm	BCV63	S7	Mm	BCY71	S3	Sm
BC549	S3	Sm	BCV64	S7	Mm	BCY72	S3	Sm
BC550	S3	Sm	BCV65	S7	Mm	BCY78	S3	Sm
BC556	S3	Sm	BCV71;R	S7	Mm	BCY79	S3	Sm
BC557	S3	Sm	BCV72;R	S7	Mm	BCY87	S3	Sm
BC558	S3	Sm	BCW29;R	S7	Mm	BCY88	S3	Sm
BC559	S3	Sm	BCW30;R	S7	Mm	BCY89	S3	Sm
BC560	S3	Sm	BCW31;R	S7	Mm	BD131	S4a	P
BC635	S3	Sm	BCW32;R	S7	Mm	BD132	S4a	P
BC636	S3	Sm	BCW33;R	S7	Mm	BD135	S4a	P
BC637	S3	Sm	BCW60*	S7	Mm	BD136	S4a	P
BC638	S3	Sm	BCW61*	S7	Mm	BD137	S4a	P

* = series

FET = Field-effect transistors

Mm = Microminiature semiconductors
for hybrid circuits

P = Low-frequency power transistors

Sm = Small-signal transistors

T = Tuner diodes

type no.	book	section	type no.	book	section	type no.	book	section
BD138	S4a	P	BD244A	S4a	P	BD816	S4a	P
BD139	S4a	P	BD244B	S4a	P	BD817	S4a	P
BD140	S4a	P	BD244C	S4a	P	BD818	S4a	P
BD201	S4a	P	BD329	S4a	P	BD825	S4a	P
BD202	S4a	P	BD330	S4a	P	BD826	S4a	P
BD203	S4a	P	BD331	S4a	P	BD827	S4a	P
BD204	S4a	P	BD332	S4a	P	BD828	S4a	P
BD226	S4a	P	BD333	S4a	P	BD829	S4a	P
BD227	S4a	P	BD334	S4a	P	BD830	S4a	P
BD228	S4a	P	BD335	S4a	P	BD839	S4a	P
BD229	S4a	P	BD336	S4a	P	BD840	S4a	P
BD230	S4a	P	BD337	S4a	P	BD841	S4a	P
BD231	S4a	P	BD338	S4a	P	BD842	S4a	P
BD233	S4a	P	BD433	S4a	P	BD843	S4a	P
BD234	S4a	P	BD434	S4a	P	BD844	S4a	P
BD235	S4a	P	BD435	S4a	P	BD845	S4a	P
BD236	S4a	P	BD436	S4a	P	BD846	S4a	P
BD237	S4a	P	BD437	S4a	P	BD847	S4a	P
BD238	S4a	P	BD438	S4a	P	BD848	S4a	P
BD239	S4a	P	BD645	S4a	P	BD849	S4a	P
BD239A	S4a	P	BD646	S4a	P	BD850	S4a	P
BD239B	S4a	P	BD647	S4a	P	BD933	S4a	P
BD239C	S4a	P	BD648	S4a	P	BD934	S4a	P
BD240	S4a	P	BD649	S4a	P	BD935	S4a	P
BD240A	S4a	P	BD650	S4a	P	BD936	S4a	P
BD240B	S4a	P	BD651	S4a	P	BD937	S4a	P
BD240C	S4a	P	BD652	S4a	P	BD938	S4a	P
BD241	S4a	P	BD675	S4a	P	BD939	S4a	P
BD241A	S4a	P	BD676	S4a	P	BD940	S4a	P
BD241B	S4a	P	BD677	S4a	P	BD941	S4a	P
BD241C	S4a	P	BD678	S4a	P	BD942	S4a	P
BD242	S4a	P	BD679	S4a	P	BD943	S4a	P
BD242A	S4a	P	BD680	S4a	P	BD944	S4a	P
BD242B	S4a	P	BD681	S4a	P	BD945	S4a	P
BD242C	S4a	P	BD682	S4a	P	BD946	S4a	P
BD243	S4a	P	BD683	S4a	P	BD947	S4a	P
BD243A	S4a	P	BD684	S4a	P	BD948	S4a	P
BD243B	S4a	P	BD813	S4a	P	BD949	S4a	P
BD243C	S4a	P	BD814	S4a	P	BD950	S4a	P
BD244	S4a	P	BD815	S4a	P	BD951	S4a	P

P = Low-frequency power transistors

type no.	book	section	type no.	book	section	type no.	book	section
BD952	S4a	P	BDT60A	S4a	P	BDV64C	S4a	P
BD953	S4a	P	BDT60B	S4a	P	BDV65	S4a	P
BD954	S4a	P	BDT60C	S4a	P	BDV65A	S4a	P
BD955	S4a	P	BDT61	S4a	P	BDV65B	S4a	P
BD956	S4a	P	BDT61A	S4a	P	BDV65C	S4a	P
BDT20	S4a	P	BDT61B	S4a	P	BDV66A	S4a	P
BDT21	S4a	P	BDT61C	S4a	P	BDV66B	S4a	P
BDT29	S4a	P	BDT62	S4a	P	BDV66C	S4a	P
BDT29A	S4a	P	BDT62A	S4a	P	BDV66D	S4a	P
BDT29B	S4a	P	BDT62B	S4a	P	BDV67A	S4a	P
BDT29C	S4a	P	BDT62C	S4a	P	BDV67B	S4a	P
BDT30	S4a	P	BDT63	S4a	P	BDV67C	S4a	P
BDT30A	S4a	P	BDT63A	S4a	P	BDV67D	S4a	P
BDT30B	S4a	P	BDT63B	S4a	P	BDV91	S4a	P
BDT30C	S4a	P	BDT63C	S4a	P	BDV92	S4a	P
BDT31	S4a	P	BDT64	S4a	P	BDV93	S4a	P
BDT31A	S4a	P	BDT64A	S4a	P	BDV94	S4a	P
BDT31B	S4a	P	BDT64B	S4a	P	BDV95	S4a	P
BDT31C	S4a	P	BDT64C	S4a	P	BDV96	S4a	P
BDT32	S4a	P	BDT65	S4a	P	BDW55	S4a	P
BDT32A	S4a	P	BDT65A	S4a	P	BDW56	S4a	P
BDT32B	S4a	P	BDT65B	S4a	P	BDW57	S4a	P
BDT32C	S4a	P	BDT65C	S4a	P	BDW58	S4a	P
BDT41	S4a	P	BDT81	S4a	P	BDW59	S4a	P
BDT41A	S4a	P	BDT82	S4a	P	BDW60	S4a	P
BDT41B	S4a	P	BDT83	S4a	P	BDX35	S4a	P
BDT41C	S4a	P	BDT84	S4a	P	BDX36	S4a	P
BDT42	S4a	P	BDT85	S4a	P	BDX37	S4a	P
BDT42A	S4a	P	BDT86	S4a	P	BDX42	S4a	P
BDT42B	S4a	P	BDT87	S4a	P	BDX43	S4a	P
BDT42C	S4a	P	BDT88	S4a	P	BDX44	S4a	P
BDT51	S4a	P	BDT91	S4a	P	BDX45	S4a	P
BDT52	S4a	P	BDT92	S4a	P	BDX46	S4a	P
BDT53	S4a	P	BDT93	S4a	P	BDX47	S4a	P
BDT54	S4a	P	BDT94	S4a	P	BDX62	S4a	P
BDT55	S4a	P	BDT95	S4a	P	BDX62A	S4a	P
BDT56	S4a	P	BDT96	S4a	P	BDX62B	S4a	P
BDT57	S4a	P	BDV64	S4a	P	BDX62C	S4a	P
BDT58	S4a	P	BDV64A	S4a	P	BDX63	S4a	P
BDT60	S4a	P	BDV64B	S4a	P	BDX63A	S4a	P

P = Low-frequency power transistors

type no.	book	section	type no.	book	section	type no.	book	section
BDX63B	S4a	P	BF240	S3	Sm	BF513	S7/S5	Mm/FET
BDX63C	S4a	P	BF241	S3	Sm	BF536	S7	Mm
BDX64	S4a	P	BF245A	S5	FET	BF550;R	S7	Mm
BDX64A	S4a	P	BF245B	S5	FET	BF569	S7	Mm
BDX64B	S4a	P	BF245C	S5	FET	BF570	S7	Mm
BDX64C	S4a	P	BF247A	S5	FET	BF579	S7	Mm
BDX65	S4a	P	BF247B	S5	FET	BF583	S4b	HVP
BDX65A	S4a	P	BF247C	S5	FET	BF585	S4b	HVP
BDX65B	S4a	P	BF256A	S5	FET	BF587	S4b	HVP
BDX65C	S4a	P	BF256B	S5	FET	BF591	S4b	HVP
BDX66	S4a	P	BF256C	S5	FET	BF593	S4b	HVP
BDX66A	S4a	P	BF324	S3	Sm	BF620	S7	Mm
BDX66B	S4a	P	BF370	S3	Sm	BF621	S7	Mm
BDX66C	S4a	P	BF410A	S5	FET	BF622	S7	Mm
BDX67	S4a	P	BF410B	S5	FET	BF623	S7	Mm
BDX67A	S4a	P	BF410C	S5	FET	BF660;R	S7	Mm
BDX67B	S4a	P	BF410D	S5	FET	BF689K	S10	WBT
BDX67C	S4a	P	BF419	S4b	HVP	BF763	S10	WBT
BDX68	S4a	P	BF420	S3	Sm	BF767	S7	Mm
BDX68A	S4a	P	BF421	S3	Sm	BF819	S4b	HVP
BDX68B	S4a	P	BF422	S3	Sm	BF820	S7	Mm
BDX68C	S4a	P	BF423	S3	Sm	BF821	S7	Mm
BDX69	S4a	P	BF450	S3	Sm	BF822	S7	Mm
BDX69A	S4a	P	BF451	S3	Sm	BF823	S7	Mm
BDX69B	S4a	P	BF457	S4b	HVP	BF824	S7	Mm
BDX69C	S4a	P	BF458	S4b	HVP	BF840	S7	Mm
BDX77	S4a	P	BF459	S4b	HVP	BF841	S7	Mm
BDX78	S4a	P	BF469	S4b	HVP	BF857	S4b	HVP
BDX91	S4a	P	BF470	S4b	HVP	BF858	S4b	HVP
BDX92	S4a	P	BF471	S4b	HVP	BF859	S4b	HVP
BDX93	S4a	P	BF472	S4b	HVP	BF869	S4b	HVP
BDX94	S4a	P	BF483	S3	Sm	BF870	S4b	HVP
BDX95	S4a	P	BF485	S3	Sm	BF871	S4b	HVP
BDX96	S4a	P	BF487	S3	Sm	BF872	S4b	HVP
BDY90	S4a	P	BF494	S3	Sm	BF926	S3	Sm
BDY90A	S4a	P	BF495	S3	Sm	BF936	S3	Sm
BDY91	S4a	P	BF496	S3	Sm	BF939	S3	Sm
BDY92	S4a	P	BF510	S7/S5	Mm/FET	BF960	S5	FET
BF198	S3	Sm	BF511	S7/S5	Mm/FET	BF964	S5	FET
BF199	S3	Sm	BF512	S7/S5	Mm/FET	BF966	S5	FET

FET = Field-effect transistors
HVP = High-voltage power transistors
Mm = Micronature semiconductors
for hybrid circuits

P = Low-frequency power transistors
Sm = Small-signal transistors
WBT = Wideband transistors

type no.	book	section	type no.	book	section	type no.	book	section
BF967	S3	Sm	BFQ19	S7/S10	Mm/WBT	BFR92A	S7/S10	Mm
BF970	S3	Sm	BFQ22S	S10	WBT	BFR93	S7/S10	Mm/WBT
BF970A	S3	Sm	BFQ23	S10	WBT	BFR93A	S7/S10	Mm/WBT
BF979	S3	Sm	BFQ23C	S10	WBT	BFR94	S10	WBT
BF980	S5	FET	BFQ24	S10	WBT	BFR95	S10	WBT
BF981	S5	FET	BFQ32	S10	WBT	BFR96	S10	WBT
BF982	S5	FET	BFQ32C	S10	WBT	BFR96S	S10	WBT
BF989	S7/S5	Mm/FET	BFQ32M	S10	WBT	BFR101A;B	S7/S5	Mm/FET
BF990	S7/S5	Mm/FET	BFQ32S	S10	WBT	BFS17	S7/S10	Mm/WBT
BF991	S7/S5	Mm/FET	BFQ33	S10	WBT	BFS17A	S10	WBT
BF992	S7/S5	Mm/FET	BFQ33C	S10	WBT	BFS18;R	S7	Mm
BF994	S7/S5	Mm/FET	BFQ34	S10	WBT	BFS19;R	S7	Mm
BF994S	S7	Mm/FET	BFQ34T	S10	WBT	BFS20;R	S7	Mm
BF996	S7/S5	Mm/FET	BFQ42	S6	RFP	BFS21	S5	FET
BF996S	S7	Mm/FET	BFQ43	S6	RFP	BFS21A	S5	FET
BF997	S7	Mm/FET	BFQ43S	S6	RFP	BFS22A	S6	RFP
BFG23	S10	WBT	BFQ51	S10	WBT	BFS23A	S6	RFP
BFG32	S10	WBT	BFQ51C	S10	WBT	BFT24	S10	WBT
BFG34	S10	WBT	BFQ52	S10	WBT	BFT25	S7/S10	Mm/WBT
BFG51	S10	WBT	BFQ53	S10	WBT	BFT25R	S7	Mm
BFG65	S10	WBT	BFQ63	S10	WBT	BFT44	S3	Sm
BFG67	S7/S10	Mm	BFQ65	S10	WBT	BFT45	S3	Sm
BFG90A	S10	WBT	BFQ66	S10	WBT	BFT46	S7/S5	Mm/FET
BFG91A	S10	WBT	BFQ67	S7/S10	Mm/WBT	BFT92	S7/S10	Mm/WBT
BFG92A	S10	WBT	BFQ68	S10	WBT	BFT93	S7/S10	Mm/WBT
BFG93A	S10	WBT	BFQ136	S10	WBT	BFW10	S5	FET
BFG96	S10	WBT	BFR29	S5	FET	BFW11	S5	FET
BFG195	S10	WBT	BFR30	S7/S5	Mm/FET	BFW12	S5	FET
BFP90A	S10	WBT	BFR31	S7/S5	Mm/FET	BFW13	S5	FET
BFP91A	S10	WBT	BFR49	S10	WBT	BFW16A	S10	WBT
BFP96	S10	WBT	BFR53	S7/S10	Mm/WBT	BFW17A	S10	WBT
BFQ10	S5	FET	BFR54	S3	Sm	BFW30	S10	WBT
BFQ11	S5	FET	BFR64	S10	WBT	BFW61	S5	FET
BFQ12	S5	FET	BFR65	S10	WBT	BFW92	S10	WBT
BFQ13	S5	FET	BFR84	S5	FET	BFW92A	S10	WBT
BFQ14	S5	FET	BFR90	S10	WBT	BFW93	S10	WBT
BFQ15	S5	FET	BFR90A	S10	WBT	BFX34	S3	Sm
BFQ16	S5	FET	BFR91	S10	WBT	BFX89	S10	WBT
BFQ17	S7/S10	Mm/WBT	BFR91A	S10	WBT	BFY50	S3	Sm
BFQ18A	S7/S10	Mm/WBT	BFR92	S7/S10	Mm/WBT	BFY51	S3	Sm

* = series

FET = Field-effect transistors

Mm = Microminiature semiconductors
for hybrid circuits

RFP = R.F. power transistors and modules

RT = Tripler

Sm = Small-signal transistors

ThM = Thyristor modules

WBM = Wideband hybrid IC modules

WBT = Wideband transistors

type no.	book	section	type no.	book	section	type no.	book	section
BFY52	S3	Sm	BGY58A	S10	WBM	BLU45/12	S6	RFP
BFY55	S3	Sm	BGY59	S10	WBM	BLU50	S6	RFP
BFY90	S10	WBT	BGY60	S10	WBM	BLU51	S6	RFP
BG2000	S1	RT	BGY61	S10	WBM	BLU52	S6	RFP
BG2097	S1	RT	BGY65	S10	WBM	BLU53	S6	RFP
BGD102	S10	WBM	BGY67	S10	WBM	BLU60/12	S6	RFP
BGD102E	S10	WBM	BGY67A	S10	WBM	BLU97	S6	RFP
BGD104	S10	WBM	BGY70	S10	WBM	BLU98	S6	RFP
BGD104E	S10	WBM	BGY71	S10	WBM	BLU99	S6	RFP
BGD502	S10	WBM	BGY74	S10	WBM	BLV10	S6	RFP
BGD504	S10	WBM	BGY75	S10	WBM	BLV11	S6	RFP
BGX885	S10	WBM	BGY78	S10	WBM	BLV20	S6	RFP
BGY22	S6	RFP	BGY84	S10	WBM	BLV21	S6	RFP
BGY22A	S6	RFP	BGY84A	S10	WBM	BLV25	S6	RFP
BGY23	S6	RFP	BGY85	S10	WBM	BLV30	S6	RFP
BGY23A	S6	RFP	BGY85A	S10	WBM	BLV30/12	S6	RFP
BGY32	S6	RFP	BGY86	S10	WBM	BLV31	S6	RFP
BGY33	S6	RFP	BGY87	S10	WBM	BLV32F	S6	RFP
BGY35	S6	RFP	BGY88	S10	WBM	BLV33	S6	RFP
BGY36	S6	RFP	BGY90A	S6	RFP	BLV33F	S6	RFP
BGY40A	S6	RFP	BGY90B	S6	RFP	BLV36	S6	RFP
BGY40B	S6	RFP	BGY93 *	S6	RFP	BLV45/12	S6	RFP
BGY41A	S6	RFP	BGY94 *	S6	RFP	BLV57	S6	RFP
BGY41B	S6	RFP	BGY95A	S6	RFP	BLV59	S6	RFP
BGY43	S6	RFP	BGY95B	S6	RFP	BLV75/12	S6	RFP
BGY45A	S6	RFP	BGY96A	S6	RFP	BLV80/28	S6	RFP
BGY45B	S6	RFP	BGY96B	S6	RFP	BLV90	S6	RFP
BGY46A	S6	RFP	BGY584A	S10	WBM	BLV90/SL	S6	RFP
BGY46B	S6	RFP	BGY585A	S10	WBM	BLV91	S6	RFP
BGY47 *	S6	RFP	BGY586	S10	WBM	BLV91/SL	S6	RFP
BGY48 *	S6	RFP	BGY587	S10	WBM	BLV92	S6	RFP
BGY50	S10	WBM	BLF146	S6	RFP/FET	BLV93	S6	RFP
BGY51	S10	WBM	BLF242	S6	RFP/FET	BLV94	S6	RFP
BGY52	S10	WBM	BLF244	S6	RFP/FET	BLV95	S6	RFP
BGY53	S10	WBM	BLF245	S6	RFP/FET	BLV97	S6	RFP
BGY54	S10	WBM	BLT90/SL	S6	RFP	BLV98	S6	RFP
BGY55	S10	WBM	BLT91/SL	S6	RFP	BLV99	S6	RFP
BGY56	S10	WBM	BLT92/SL	S6	RFP	BLW29	S6	RFP
BGY57	S10	WBM	BLU20/12	S6	RFP	BLW31	S6	RFP
BGY58	S10	WBM	BLU30/12	S6	RFP	BLW32	S6	RFP

* = series

FET = Field-effect transistors

RFP = R.F. power transistors and modules

ThM = Thyristor modules

WBM = Wideband hybrid IC modules

type no.	book	section	type no.	book	section	type no.	book	section
BLW33	S6	RFP	BLX94C	S6	RFP	BRY52	S7	Mm
BLW34	S6	RFP	BLX95	S6	RFP	BS107	S5	FET
BLW50F	S6	RFP	BLX96	S6	RFP	BS170	S5	FET
BLW60	S6	RFP	BLX97	S6	RFP	BSD10	S5	FET
BLW60C	S6	RFP	BLX98	S6	RFP	BSD12	S5	FET
BLW76	S6	RFP	BLY87A	S6	RFP	BSD20	S5/7	FET
BLW77	S6	RFP	BLY87C	S6	RFP	BSD22	S5/7	FET
BLW78	S6	RFP	BLY88A	S6	RFP	BSD212	S5	FET
BLW79	S6	RFP	BLY88C	S6	RFP	BSD213	S5	FET
BLW80	S6	RFP	BLY89A	S6	RFP	BSD214	S5	FET
BLW81	S6	RFP	BLY89C	S6	RFP	BSD215	S5	FET
BLW83	S6	RFP	BLY90	S6	RFP	BSR12;R	S7	Mm
BLW84	S6	RFP	BLY91A	S6	RFP	BSR13;R	S7	Mm
BLW85	S6	RFP	BLY91C	S6	RFP	BSR14;R	S7	Mm
BLW86	S6	RFP	BLY92A	S6	RFP	BSR15;R	S7	Mm
BLW87	S6	RFP	BLY92C	S6	RFP	BSR16;R	S7	Mm
BLW89	S6	RFP	BLY93A	S6	RFP	BSR17;R	S7	Mm
BLW90	S6	RFP	BLY93C	S6	RFP	BSR17A;R	S7	Mm
BLW91	S6	RFP	BLY94	S6	RFP	BSR18;R	S7	Mm
BLW95	S6	RFP	BPF24	S8b	PDT	BSR18A;R	S7	Mm
BLW96	S6	RFP	BPW22A	S8a/b	PDT	BSR19; A	S7	Mm
BLW97	S6	RFP	BPW50	S8a/b	PDT	BSR20; A	S7	Mm
BLW98	S6	RFP	BPW71	S8b	PDT	BSR30	S7	Mm
BLW99	S6	RFP	BPX25	S8b	PDT	BSR31	S7	Mm
BLX13	S6	RFP	BPX29	S8b	PDT	BSR32	S7	Mm
BLX13C	S6	RFP	BPX40	S8b	PDT	BSR33	S7	Mm
BLX14	S6	RFP	BPX41	S8b	PDT	BSR40	S7	Mm
BLX15	S6	RFP	BPX42	S8b	PDT	BSR41	S7	Mm
BLX39	S6	RFP	BPX61	S8b	PDT	BSR42	S7	Mm
BLX65	S6	RFP	BPX61P	S8b	PDT	BSR43	S7	Mm
BLX65E	S6	RFP	BPX71	S8b	PDT	BSR50	S3	Sm
BLX65ES	S6	RFP	BPX72	S8b	PDT	BSR51	S3	Sm
BLX67	S6	RFP	BR100/03	S2b	Th	BSR52	S3	Sm
BLX68	S6	RFP	BR101	S3	Sm	BSR55	S7/S5	Mm/FET
BLX69A	S6	RFP	BR210*	S2a	Th	BSR57	S7/S5	Mm/FET
BLX91A	S6	RFP	BR216*	S2a	Th	BSR58	S7/S5	Mm/FET
BLX91CB	S6	RFP	BR220*	S2a	Th	BSR60	S3	Sm
BLX92A	S6	RFP	BRY39	S3	Sm	BSR61	S3	Sm
BLX93A	S6	RFP	BRY56	S3	Sm	BSR62	S3	Sm
BLX94A	S6	RFP	BRY61	S7	Mm	BSS38	S3	Sm

FET = Field-effect transistors

Mm = Microminiature semiconductors
for hybrid circuits

PDT = Photodiodes or transistors

RFP = R.F. power transistors and modules

Sm = Small-signal transistors

Th = Thyristors

type no.	book	section	type no.	book	section	type no.	book	section
BSS50	S3	Sm	BSV78	S5	FET	BTW60D*	S2b	Th
BSS51	S3	Sm	BSV79	S5	FET	BTW70*	S2b	Th
BSS52	S3	Sm	BSV80	S5	FET	BTW70D*	S2b	Th
BSS60	S3	Sm	BSV81	S5	FET	BTW23*	S2b	Th
BSS61	S3	Sm	BSW66A	S3	Sm	BTW38*	S2b	Th
BSS62	S3	Sm	BSW67A	S3	Sm	BTW40*	S2b	Th
BSS63;R	S7	Mm	BSW68A	S3	Sm	BTW42*	S2b	Th
BSS64;R	S7	Mm	BSX19	S3	Sm	BTW43*	S2b	Tri
BSS68	S3	Sm	BSX20	S3	Sm	BTW45*	S2b	Th
BSS83	S5/7	FET/Mm	BSX32	S3	Sm	BTW58*	S2b	Th
BST15	S7	Mm	BSX45	S3	Sm	BTW62*	S2b	Th
BST16	S7	Mm	BSX46	S3	Sm	BTW62D*	S2b	Th
BST39	S7	Mm	BSX47	S3	Sm	BTW63*	S2b	Th
BST40	S7	Mm	BSX59	S3	Sm	BTY79*	S2b	Th
BST50	S7	Mm	BSX60	S3	Sm	BTY91*	S2b	Th
BST51	S7	Mm	BSX61	S3	Sm	BU426	S4b	SP
BST52	S7	Mm	BT136*	S2b	Tri	BU426A	S4b	SP
BST60	S7	Mm	BT136F*	S2b	Tri	BU433	S4b	SP
BST61	S7	Mm	BT137*	S2b	Tri	BU505	S4b	SP
BST62	S7	Mm	BT137F*	S2b	Tri	BU506	S4b	SP
BST70A	S5	FET	BT138*	S2b	Tri	BU506D	S4b	SP
BST72A	S5	FET	BT138F*	S2b	Tri	BU508A	S4b	SP
BST74A	S5	FET	BT139*	S2b	Tri	BU508D	S4b	SP
BST76A	S5	FET	BT139F*	S2b	Tri	BU705	S4b	SP
BST78	S5	FET	BT145*	S2b	Tri	BU706	S4b	SP
BST80	S5/S7	FET/Mm	BT149*	S2b	Th	BU706D	S4b	SP
BST82	S5/S7	FET/Mm	BT150	S2b	Th	BU806	S4b	SP
BST84	S5/S7	FET/Mm	BT151*	S2b	Th	BU807	S4b	SP
BST86	S5/S7	FET/Mm	BT151F*	S2b	Th	BU808	S4b	SP
BST90	S5	FET	BT152*	S2b	Th	BU824	S4b	SP
BST97	S5	FET	BT153	S2b	Th	BU826	S4b	SP
BST100	S5	FET	BT157*	S2b	Th	BUP22*	S4b	SP
BST110	S5	FET	BT169*	S2b	Th	BUP23*	S4b	SP
BST120	S5/S7	FET/Mm	BT1140*	S2b	Tri	BUS11;A	S4b	SP
BST122	S5/S7	FET/Mm	BTR59*	S2b	Tri	BUS12;A	S4b	SP
BSV15	S3	Sm	BTS59*	S2b	Tri	BUS13;A	S4b	SP
BSV16	S3	Sm	BTW58*	S2b	Th	BUS14;A	S4b	SP
BSV17	S3	Sm	BTW59*	S2b	Th	BUS21*	S4b	SP
BSV52;R	S7	Mm	BTW59D*	S2b	Th	BUS22*	S4b	SP
BSV64	S3	Sm	BTW60*	S2b	Th	BUS23*	S4b	SP

* = series

FET = Field-effect transistors

Mm = Microminiature semiconductors
for hybrid circuits

Sm = Small-signal transistors

SP = Low-frequency switching power transistors

Th = Thyristors

Tri = Triacs

INDEX

type no.	book	section	type no.	book	section	type no.	book	section
BUT11;A	S4b	SP	BUZ25	S9	PM	BUZ211	S9	PM
BUT11A	S4b	SP	BUZ31	S9	PM	BUZ307	S9	PM
BUT11AF	S4b	SP	BUZ32	S9	PM	BUZ308	S9	PM
BUV82	S4b	SP	BUZ34	S9	PM	BUZ310	S9	PM
BUV83	S4b	SP	BUZ35	S9	PM	BUZ311	S9	PM
BUV89	S4b	SP	BUZ36	S9	PM	BUZ326	S9	PM
BUV90;A	S4b	SP	BUZ41A	S9	PM	BUZ330	S9	PM
BUW11;A	S4b	SP	BUZ42	S9	PM	BUZ331	S9	PM
BUW12;A	S4b	SP	BUZ45	S9	PM	BUZ347	S9	PM
BUW13;A	S4b	SP	BUZ45A	S9	PM	BUZ348	S9	PM
BUW84	S4b	SP	BUZ45B	S9	PM	BUZ349	S9	PM
BUW85	S4b	SP	BUZ50A	S9	PM	BUZ350	S9	PM
BUX46;A	S4b	SP	BUZ50B	S9	PM	BUZ351	S9	PM
BUX47;A	S4b	SP	BUZ50C	S9	PM	BUZ355	S9	PM
BUX48;A	S4b	SP	BUZ53A	S9	PM	BUZ356	S9	PM
BUX80	S4b	SP	BUZ54	S9	PM	BUZ357	S9	PM
BUX81	S4b	SP	BUZ54A	S9	PM	BUZ358	S9	PM
BUX82	S4b	SP	BUZ60	S9	PM	BUZ384	S9	PM
BUX83	S4b	SP	BUZ63	S9	PM	BUZ385	S9	PM
BUX84	S4b	SP	BUZ64	S9	PM	BY224*	S2a	R
BUX84F	S4b	SP	BUZ71	S9	PM	BY225*	S2a	R
BUX85	S4b	SP	BUZ71A	S9	PM	BY228	S1	R
BUX85F	S4b	SP	BUZ72	S9	PM	BY229*	S2a	R
BUX86	S4b	SP	BUZ72A	S9	PM	BY229F*	S2a	R
BUX87	S4b	SP	BUZ73	S9	PM	BY249*	S2a	R
BUX88	S4b	SP	BUZ73A	S9	PM	BY260*	S2a	R
BUX90	S4b	SP	BUZ74	S9	PM	BY261*	S2a	R
BUX98	S4b	SP	BUZ74A	S9	PM	BY329*	S2a	R
BUX98A	S4b	SP	BUZ76	S9	PM	BY359*	S2a	R
BUX99	S4b	SP	BUZ76A	S9	PM	BY438	S1	R
BUY89	S4b	SP	BUZ78	S9	PM	BY448	S1	R
BUZ10	S9	PM	BUZ80	S9	PM	BY458	S1	R
BUZ11	S9	PM	BUZ80A	S9	PM	BY505	S1	R
BUZ11A	S9	PM	BUZ83	S9	PM	BY509	S1	R
BUZ14	S9	PM	BUZ83A	S9	PM	BY527	S1	R
BUZ15	S9	PM	BUZ84	S9	PM	BY584	S1	R
BUZ20	S9	PM	BUZ84A	S9	PM	BY588	S1	R
BUZ21	S9	PM	BUZ90	S9	PM	BY609	S1	R
BUZ23	S9	PM	BUZ90A	S9	PM	BY610	S1	R
BUZ24	S9	PM	BUZ94	S9	PM	BY614	S1	R

* = series

PM = Power MOS transistors

R = Rectifier diodes

SP = Low-frequency switching power transistors

type no.	book	section	type no.	book	section	type no.	book	section
BY619	S1	R	BYV28*	S1/S2a	R	BYW96D	S1	R
BY620	S1	R	BYV29*	S2a	R	BYW96E	S1	R
BY627	S1	R	BYV29F*	S2a	R	BYX10G	S1	R
BY707	S1	R	BYV30*	S2a	R	BYX25*	S2a	R
BY708	S1	R	BYV31*	S2a	R	BYX30*	S2a	R
BY709	S1	R	BYV32*	S2a	R	BYX32*	S2a	R
BY710	S1	R	BYV32F*	S2a	R	BYX38*	S2a	R
BY711	S1	R	BYV33*	S2a	R	BYX39*	S2a	R
BY712	S1	R	BYV33F*	S2a	R	BYX42*	S2a	R
BY713	S1	R	BYV34*	S2a	R	BYX46*	S2a	R
BY714	S1	R	BYV36 *	S1	R	BYX50*	S2a	R
BYD13 *	S1	R	BYV39*	S2a	R	BYX52*	S2a	R
BYD14 *	S1	R	BYV42*	S2a	R	BYX56*	S2a	R
BYD17 *	S1/7	R	BYV43*	S2a	R	BYX90G	S1	R
BYD33 *	S1	R	BYV43F*	S2a	R	BYX96*	S2a	R
BYD37 *	S1/7	R	BYV44*	S2a	R	BYX97*	S2a	R
BYD73 *	S1	R	BYV60*	S2a	R	BYX98*	S2a	R
BYD74 *	S1	R	BYV72*	S2a	R	BYX99*	S2a	R
BYD77 *	S1	R	BYV73*	S2a	R	BZD23	S1	Vrg
BYM26 *	S1	R	BYV74*	S2a	R	BZD27	S1/7	Vrg
BYM36 *	S1	R	BYV79*	S2a	R	BZT03	S1	Vrg
BYM56 *	S1	R	BYV92*	S2a	R	BZV10	S1	Vrf
BYP21*	S2a	R	BYV95A	S1	R	BZV11	S1	Vrf
BYP22*	S2a	R	BYV95B	S1	R	BZV12	S1	Vrf
BYP59*	S2a	R	BYV95C	S1	R	BZV13	S1	Vrf
BYQ28*	S2a	R	BYV96D	S1	R	BZV14	S1	Vrf
BYR29*	S2a	R	BYV96E	S1	R	BZV37	S1	Vrf
BYR29F*	S2a	R	BYW25*	S2a	R	BZV46	S1	Vrg
BYT28*	S2a	R	BYW29*	S2a	R	BZV49*	S1/S7	Vrg/Mm
BYT79*	S2a	R	BYW29F*	S2a	R	BZV55*	S7	Mm
BYV10	S1	R	BYW30*	S2a	R	BZV80	S1	Vrf
BYV18*	S2a	R	BYW31*	S2a	R	BZV81	S1	Vrf
BYV19*	S2a	R	BYW54	S1	R	BZV85 *	S1	Vrg
BYV20*	S2a	R	BYW55	S1	R	BZW03 *	S1	Vrg
BYV21*	S2a	R	BYW56	S1	R	BZW14	S1	Vrg
BYV22*	S2a	R	BYW92*	S2a	R	BZW86*	S2a	TS
BYV23*	S2a	R	BYW93*	S2a	R	BZX55 *	S1	Vrg
BYV24*	S2a	R	BYW95A	S1	R	BZX70*	S2a	Vrg
BYV26 *	S1/S2a	R	BYW95B	S1	R	BZX75 *	S1	Vrg
BYV27*	S1/S2a	R	BYW95C	S1	R	BZX79*	S1	Vrg

* = series

LED = Light-emitting diodes

M = Microwave transistors

Mm = Microminiature semiconductors
for hybrid circuits

Ph = Photoconductive devices

PhC = Photocouplers

R = Rectifier diodes

TS = Transient suppressor diodes

Vrf = Voltage reference diodes

Vrg = Voltage regulator diodes

type no.	book	section	type no.	book	section	type no.	book	section
BZX84*	S7/S1	Mm/Vrg	CNY62	S8b	PhC	CQW12B(L)S8a		LED
BZY91*	S2a	Vrg	CNY63	S8b	PhC	CQW20A	S8a	LED
BZY93*	S2a	Vrg	CQF24	S8b	Ph	CQW21	S8a	LED
CFX13	S11	M	CQL10A	S8b	Ph	CQW22	S8a	LED
CFX21	S11	M	CQL13A	S8b	Ph	CQW24(L)	S8a	LED
CFX30	S11	M	CQL16	S8b	Ph	CQW54	S8a	LED
CFX31	S11	M	CQS51L	S8a	LED	CQW60(L)	S8a	LED
CFX32	S11	M	CQS54	S8a	LED	CQW60A(L)S8a		LED
CFX33	S11	M	CQS82L	S8a	LED	CQW60U(L)S8a		LED
CNG35	S8b	PhC	CQS82AL	S8a	LED	CQW61(L)	S8a	LED
CNG36	S8b	PhC	CQS84L	S8a	LED	CQW62(L)	S8a	LED
CNR36	S8b	PhC	CQS86L	S8a	LED	CQW89A	S8a/b	I
CNX21	S8b	PhC	CQS93	S8a	LED	CQW93	S8a	LED
CNX35	S8b	PhC	CQS93E	S8a	LED	CQW95	S8a	LED
CNX35U	S8b	PhC	CQS93L	S8a	LED	CQW97	S8a	LED
CNX36	S8b	PhC	CQS95	S8a	LED	CQX24(L)	S8a	LED
CNX36U	S8b	PhC	CQS95E	S8a	LED	CQX51(L)	S8a	LED
CNX38	S8b	PhC	CQS95L	S8a	LED	CQX54(L)	S8a	LED
CNX38U	S8b	PhC	CQS97	S8a	LED	CQX54D	S8a	LED
CNX39	S8b	PhC	CQS97E	S8a	LED	CQX64(L)	S8a	LED
CNX39U	S8b	PhC	CQS97L	S8a	LED	CQX64D	S8a	LED
CNX44	S8b	PhC	CQT10B	S8a	LED	CQX74(L)	S8a	LED
CNX44A	S8b	PhC	CQT24	S8a	LED	CQX74D	S8a	LED
CNX46	S8b	PhC	CQT60	S8a	LED	CQY11B	S8b	LED
CNX48	S8b	PhC	CQT70	S8a	LED	CQY11C	S8b	LED
CNX48U	S8b	PhC	CQT80L	S8a	LED	CQY24B(L)S8a		LED
CNX62	S8b	PhC	CQV70(L)	S8a	LED	CQY49B	S8b	LED
CNX72	S8b	PhC	CQV70A(L)S8a		LED	CQY49C	S8b	LED
CNX82	S8b	PhC	CQV70U(L)S8a		LED	CQY50	S8b	LED
CNX83	S8b	PhC	CQV71A(L)S8a		LED	CQY52	S8b	LED
CNX91	S8b	PhC	CQV72(L)	S8a	LED	CQY53S	S8b	LED
CNX92	S8b	PhC	CQV80L	S8a	LED	CQY54A	S8a	LED
CNY17-1	S8b	PhC	CQV80AL	S8a	LED	CQY58A	S8a/b	I
CNY17-2	S8b	PhC	CQV80UL	S8a	LED	CQY89A	S8a/b	I
CNY17-3	S8b	PhC	CQV81L	S8a	LED	CQY94B(L)S8a		LED
CNY50	S8b	PhC	CQV82L	S8a	LED	CQY95B	S8a	LED
CNY57	S8b	PhC	CQW10A(L)S8a		LED	CQY96(L)	S8a	LED
CNY57A	S8b	PhC	CQW10B(L)S8a		LED	CQY97A	S8a	LED
CNY57AU	S8b	PhC	CQW10U(L)S8a		LED	Fresnel-	S8b	A
CNY57U	S8b	PhC	CQW11B(L)S8a		LED	lens		

* = series

A = Accessories

I = Infrared devices

LED = Light-emitting diodes

M = Microwave transistors

PhC = Photocouplers

SEN = Sensors

type no.	book	section	type no.	book	section	type no.	book	section
H11A1	S8b	PhC	LKE21004R	S11	M	MPSA13	S3	Sm
H11A2	S8b	PhC	LKE21015T	S11	M	MPSA14	S3	Sm
H11A3	S8b	PhC	LKE21050T	S11	M	MPSA42	S3	Sm
H11A4	S8b	PhC	LKE27010R	S11	M	MPSA43	S3	Sm
H11A5	S8b	PhC	LKE27025R	S11	M	MPSA55	S3	Sm
H11B1	S8b	PhC	LKE32002T	S11	M	MPSA56	S3	Sm
H11B2	S8b	PhC	LKE32004T	S11	M	MPSA63	S3	Sm
H11B3	S8b	PhC	LTE42005S	S11	M	MPSA64	S3	Sm
H11B255	S8b	PhC	LTE42008R	S11	M	MPSA92	S3	Sm
KMZ10A	S13	SEN	LTE42012R	S11	M	MPSA93	S3	Sm
KMZ10B	S13	SEN	LV1721E50R	S11	M	MRB12175YR	S11	M
KMZ10C	S13	SEN	LV2024E45R	S11	M	MRB12350YR	S11	M
KP100A	S13	SEN	LV2327E40R	S11	M	MS1011B700YS11	M	M
KP101A	S13	SEN	LV3742E16R	S11	M	MS6075B800ZS11	M	M
KPZ20G	S13	SEN	LV3742E24R	S11	M	MSB12900Y	S11	M
KPZ21G	S13	SEN	LWE2015R	S11	M	MZ0912B75Y	S11	M
KTY81*	S13	SEN	LWE2025R	S11	M	MZ0912B150YS11	M	M
KTY83*	S13	SEN	LZ1418E100RS11	M		OM286; M	S13	SEN
KTY84*	S13	SEN	MCA230	S8b	PhC	OM287; M	S13	SEN
LAE2001R	S11	M	MCA231	S8b	PhC	OM320	S10	WBM
LAE4000Q	S11	M	MCA255	S8b	PhC	OM321	S10	WBM
LAE4001R	S11	M	MCT2	S8b	PhC	OM322	S10	WBM
LAE4002S	S11	M	MCT26	S8b	PhC	OM323	S10	WBM
LAE6000Q	S11	M	MKB12040WS	S11	M	OM323A	S10	WBM
LBE1004R	S11	M	MKB12100WS	S11	M	OM335	S10	WBM
LBE1010R	S11	M	MKB12140W	S11	M	OM336	S10	WBM
LBE2003S	S11	M	MO6075B200ZS11	M		OM337	S10	WBM
LBE2005Q	S11	M	MO6075B400ZS11	M		OM337A	S10	WBM
LBE2008T	S11	M	MPS6513	S3	Sm	OM339	S10	WBM
LBE2009S	S11	M	MPS6514	S3	Sm	OM345	S10	WBM
LCE1010R	S11	M	MPS6515	S3	Sm	OM350	S10	WBM
LCE2003S	S11	M	MPS6517	S3	Sm	OM360	S10	WBM
LCE2005Q	S11	M	MPS6518	S3	Sm	OM361	S10	WBM
LCE2008T	S11	M	MPS6519	S3	Sm	OM370	S10	WBM
LCE2009S	S11	M	MPS6520	S3	Sm	OM386B	S13	SEN
LJE42002T	S11	M	MPS6521	S3	Sm	OM386M	S13	SEN
LKE1004R	S11	M	MPS6522	S3	Sm	OM387B	S13	SEN
LKE2002T	S11	M	MPS6523	S3	Sm	OM387M	S13	SEN
LKE2004T	S11	M	MPSA05	S3	Sm	OM388B	S13	SEN
LKE2015T	S11	M	MPSA06	S3	Sm	OM389B	S13	SEN

FET = Field-effect transistors

I = Infrared devices

M = Microwave transistors

Mm = Microminiature semiconductors
for hybrid circuits

P = Low-frequency power transistors

PhC = Photocouplers

R = Rectifier diodes

SD = Small-signal diodes

SEN = Sensors

Sm = Small-signal transistors

SP = Low-frequency switching power transistors

St = Rectifier stacks

WBM = Wideband hybrid IC modules

type no.	book	section	type no.	book	section	type no.	book	section
RZ1214B65Y S11	M		TIP125	S4a	P	1N4003G	S1	R
RZ1214B125WS11	M		TIP126	S4a	P	1N4004G	S1	R
RZ1214B125YS11	M		TIP127	S4a	P	1N4005G	S1	R
RZ1214B150YS11	M		TIP130	S4a	P	1N4006G	S1	R
RZ2833B45W S11	M		TIP131	S4a	P	1N4007G	S1	R
RZ3135B15U S11	M		TIP132	S4a	P	1N4148	S1	SD
RZ3135B15W S11	M		TIP135	S4a	P	1N4150	S1	SD
RZ3135B25U S11	M		TIP136	S4a	P	1N4151	S1	SD
RZ3135B30W S11	M		TIP137	S4a	P	1N4153	S1	SD
RZB12100Y S11	M		TIP140	S4a	P	1N4446	S1	SD
RZB12250Y S11	M		TIP141	S4a	P	1N4448	S1	SD
RZZ1214B300YS11	M		TIP145	S4a	P	1N4531	S1	SD
SL5500 S8b	PhC		TIP146	S4a	P	1N4532	S1	SD
SL5501 S8b	PhC		TIP147	S4a	P	1N5059	S1	R
SL5502R S8b	PhC		TIP2955	S4a	P	1N5060	S1	R
SL5504 S8b	PhC		TIP3055	S4a	P	1N5061	S1	R
SL5504S S8b	PhC		1N821;A	S1	Vrf	1N5062	S1	R
SL5505S S8b	PhC		1N823;A	S1	Vrf	2N918	S10	WBT
SL5511 S8b	PhC		1N825;A	S1	Vrf	2N930	S3	Sm
TIP29* S4a	P		1N827;A	S1	Vrf	2N1613	S3	Sm
TIP30* S4a	P		1N829;A	S1	Vrf	2N1711	S3	Sm
TIP31* S4a	P		1N914	S1	SD	2N1893	S3	Sm
TIP32* S4a	P		1N916	S1	SD	2N2219	S3	Sm
TIP33* S4a	P		1N3879	S2a	R	2N2219A	S3	Sm
TIP34* S4a	P		1N3880	S2a	R	2N2222	S3	Sm
TIP41* S4a	P		1N3881	S2a	R	2N2222A	S3	Sm
TIP42* S4a	P		1N3882	S2a	R	2N2297	S3	Sm
TIP47 S4a	P		1N3883	S2a	R	2N2368	S3	Sm
TIP48 S4a	P		1N3889	S2a	R	2N2369	S3	Sm
TIP49 S4a	P		1N3890	S2a	R	2N2369A	S3	Sm
TIP50 S4a	P		1N3891	S2a	R	2N2483	S3	Sm
TIP110 S4a	P		1N3892	S2a	R	2N2484	S3	Sm
TIP111 S4a	P		1N3893	S2a	R	2N2904	S3	Sm
TIP112 S4a	P		1N3909	S2a	R	2N2904A	S3	Sm
TIP115 S4a	P		1N3910	S2a	R	2N2905	S3	Sm
TIP116 S4a	P		1N3911	S2a	R	2N2905A	S3	Sm
TIP117 S4a	P		1N3912	S2a	R	2N2906	S3	Sm
TIP120 S4a	P		1N3913	S2a	R	2N2906A	S3	Sm
TIP121 S4a	P		1N4001G	S1	R	2N2907	S3	Sm
TIP122 S4a	P		1N4002G	S1	R	2N2907A	S3	Sm

* = series

I = Infrared devices

M = Microwave transistors

P = Low-frequency power transistors

PhC = Photocouplers

R = Rectifier diodes

SD = Small-signal diodes

Vrf = Voltage reference diodes

type no.	book	section	type no.	book	section	type no.	book	section
OM931	S4a	P	PKB3005U	S11	M	PN3440	S3	Sm
OM961	S4a	P	PKB12005U	S11	M	PN5415	S3	Sm
OSB9115	S2a	St	PKB20010U	S11	M	PN5416	S3	Sm
OSB9215	S2a	St	PKB23001U	S11	M	PO44	S8b	PhC
OSB9415	S2a	St	PKB23003U	S11	M	PO44A	S8b	PhC
OSM9115	S2a	St	PKB23005U	S11	M	PPC5001T	S11	M
OSM9215	S2a	St	PKB25006T	S11	M	PQC5001T	S11	M
OSM9415	S2a	St	PKB32001U	S11	M	PTB23001X	S11	M
OSM9510	S2a	St	PKB32003U	S11	M	PTB23003X	S11	M
OSM9511	S2a	St	PKB32005U	S11	M	PTB23005X	S11	M
OSM9512	S2a	St	PMBF4391	S7	Mm	PTB32001X	S11	M
OSS9115	S2a	St	PMBF4392	S7	Mm	PTB32003X	S11	M
OSS9215	S2a	St	PMBF4393	S7	Mm	PTB32005X	S11	M
OSS9415	S2a	St	PMBT2222/A	S7	Mm	PTB42001X	S11	M
P2105	S8b	I	PMBT2907/A	S7	Mm	PTB42002X	S11	M
PBMF4391	S5	FET	PMBT3903/4	S7	Mm	PTB42003X	S11	M
PBMF4392	S5	FET	PMBT3906	S7	Mm	PV3742B4X	S11	M
PBMF4393	S5	FET	PMBT6428/9	S7	Mm	PVB42004X	S11	M
PDE1001U	S11	M	PMBTA05/06	S7	Mm	PXT3904	S7	Mm
PDE1003U	S11	M	PMBTA13/14	S7	Mm	PXT3906	S7	Mm
PDE1005U	S11	M	PMBTA42/43	S7	Mm	PZ1418B15U	S11	M
PDE1010U	S11	M	PMBTA55/56	S7	Mm	PZ1418B30U	S11	M
PEE1001U	S11	M	PMBTA63/64	S7	Mm	PZ1721B12U	S11	M
PEE1003U	S11	M	PMBTA92/93	S7	Mm	PZ1721B25U	S11	M
PEE1005U	S11	M	PMLL4148	S1	SD	PZ2024B10U	S11	M
PEE1010U	S11	M	PMLL4150	S1	SD	PZ2024B20U	S11	M
PH2222	S3	Sm	PMLL4151	S1	SD	PZB16035U	S11	M
PH2222A	S3	Sm	PMLL4153	S1	SD	PZB27020U	S11	M
PH2369	S3	Sm	PMLL4446	S1	SD	RPY97	S8b	I
PH2907	S3	Sm	PMLL4448	S1	SD	RPY100	S8b	I
PH2907A	S3	Sm	PMLL5225B			RPY101	S8b	I
PH2955T	S4a	P	to	S1/S7	SD	RPY102	S8b	I
PH3055T	S4a	P	PMLL5267B			RPY103	S8b	I
PH5415	S3	Sm	PN2222	S3	Sm	RPY107	S8b	I
PH5416	S3	Sm	PN2222A	S3	Sm	RPY109	S8b	I
PH13002	S4b	SP	PN2369	S3	Sm	RV3135B5X	S11	M
PH13003	S4b	SP	PN2369A	S3	Sm	RX1214B300YS11	M	
PHSD51	S2a	R	PN2907	S3	Sm	RXB12350Y	S11	M
PKB3001U	S11	M	PN2907A	S3	Sm	RZ1214B35Y	S11	M
PKB3003U	S11	M	PN3439	S3	Sm	RZ1214B60W	S11	M

A = Accessories
 FET = Field-effect transistors
 Ph = Photoconductive devices
 PhC = Photocouplers
 R = Rectifier diodes

RFP = R.F. power transistors and modules
 SD = Small-signal diodes
 Sm = Small-signal transistors
 WBT = Wideband transistors

type no.	book	section	type no.	book	section	type no.	book	section
2N3019	S3	Sm	2N4860	S5	FET	56354	S4b	A
2N3020	S3	Sm	2N4861	S5	FET	56359b	S2, 4b	A
2N3053	S3	Sm	2N5086	S3	Sm	56359c	S2, 4b	A
2N3375	S6	RFP	2N5087	S3	Sm	56359d	S2, 4b	A
2N3553	S6	RFP	2N5088	S3	Sm	56360a	S2, 4b	A
2N3632	S6	RFP	2N5089	S3	Sm	56363	S2, 4b	A
2N3822	S5	FET	2N5400	S3	Sm	56364	S2, 4b	A
2N3823	S5	FET	2N5401	S3	Sm	56367	S2a/b	A
2N3866	S6	RFP	2N5415	S3	Sm	56368b	S2, 4b	A
2N3903	S3	Sm	2N5416	S3	Sm	56368c	S2, 4b	A
2N3904	S3	Sm	2N5550	S3	Sm	56369	S2, 4b	A
2N3905	S3	Sm	2N5551	S3	Sm	56378	S2, 4b	A
2N3906	S3	Sm	2N6659	S5	FET	56379	S2, 4b	A
2N3924	S6	RFP	2N6660	S5	FET	56387a, b	S4b	A
2N3926	S6	RFP	2N6661	S5	FET	56397	S8b	A
2N3927	S6	RFP	4N25	S8b	PhC			
2N3966	S5	FET	4N25A	S8b	PhC			
2N4030	S3	Sm	4N26	S8b	PhC			
2N4031	S3	Sm	4N27	S8b	PhC			
2N4032	S3	Sm	4N28	S8b	PhC			
2N4033	S3	Sm	4N35	S8b	PhC			
2N4091	S5	FET	4N36	S8b	PhC			
2N4092	S5	FET	4N37	S8b	PhC			
2N4093	S5	FET	4N38	S8b	PhC			
2N4123	S3	Sm	4N38A	S8b	PhC			
2N4124	S3	Sm	502CQF	S8b	Ph			
2N4125	S3	Sm	503CQF	S8b	Ph			
2N4126	S3	Sm	504CQL	S8b	Ph			
2N4391	S5	FET	516CQF-B	S8b	Ph			
2N4392	S5	FET	56201d	S4b	A			
2N4393	S5	FET	56201j	S4b	A			
2N4400	S3	Sm	56245	S3, 10	A			
2N4401	S3	Sm	56246	S3, 10	A			
2N4402	S3	Sm	56261a	S4b	A			
2N4403	S3	Sm	56264	S2a/b	A			
2N4427	S6	RFP	56295	S2a/b	A			
2N4856	S5	FET	56326	S4b	A			
2N4857	S5	FET	56339	S4b	A			
2N4858	S5	FET	56352	S4b	A			
2N4859	S5	FET	56353	S4b	A			

A = Accessories

FET = Field-effect transistors

Ph = Photoconductive devices

PhC = Photocouplers

Sm = Small-signal diodes

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DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

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- T2a Transmitting tubes for communications, glass types**
- T2b Transmitting tubes for communications, ceramic types**
- T3 Klystrons**
- T4 Magnetrons for microwave heating**
- T5 Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications
- T6 Geiger-Müller tubes**
- T8 Colour display systems**
Colour TV picture tubes, colour data graphic display tube assemblies, deflection units
- T9 Photo and electron multipliers**
- T10 Plumbicon camera tubes and accessories**
- T11 Microwave semiconductors and components**
- T12 Vidicon and Newvicon camera tubes**
- T13 Image intensifiers and infrared detectors**
- T15 Dry reed switches**
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- S2b Thyristors and triacs**
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- S4a Low-frequency power transistors and hybrid modules**
- S4b High-voltage and switching power transistors**
- S5 Field-effect transistors**
- S6 R.F. power transistors and modules**
- S7 Surface mounted semiconductors**
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- S8b Devices for optoelectronics**
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- S9 PowerMos transistors**
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- C7 Variable capacitors
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AS56

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